Chapter 3

System Module

CONTENTS

Schematic Diagrams: UR4U – layout version 22

Transceiver NSB–1

Introduction

The NSB–1 is a radio transceiver unit for the GSM1900 network. It is a GSM phase 2 power class 4 transceiver providing 16 power levels with a maximum output power of 1W. The transceiver is true 3 V transceiver.

The transceiver consists of System/RF module (UR4U), User interface module (UE4S) and assembly parts.

The antenna is a fixed helix. External antenna connection is provided by rear RF connector

The small SIM (Subscriber Identity Module) card is located inside the phone, under the battery pack.

Functional Description

There are five different operation modes:

– power off mode

– idle mode

– active mode

– charge mode

– local mode

In the power off mode only the circuits needed for power up are supplied.

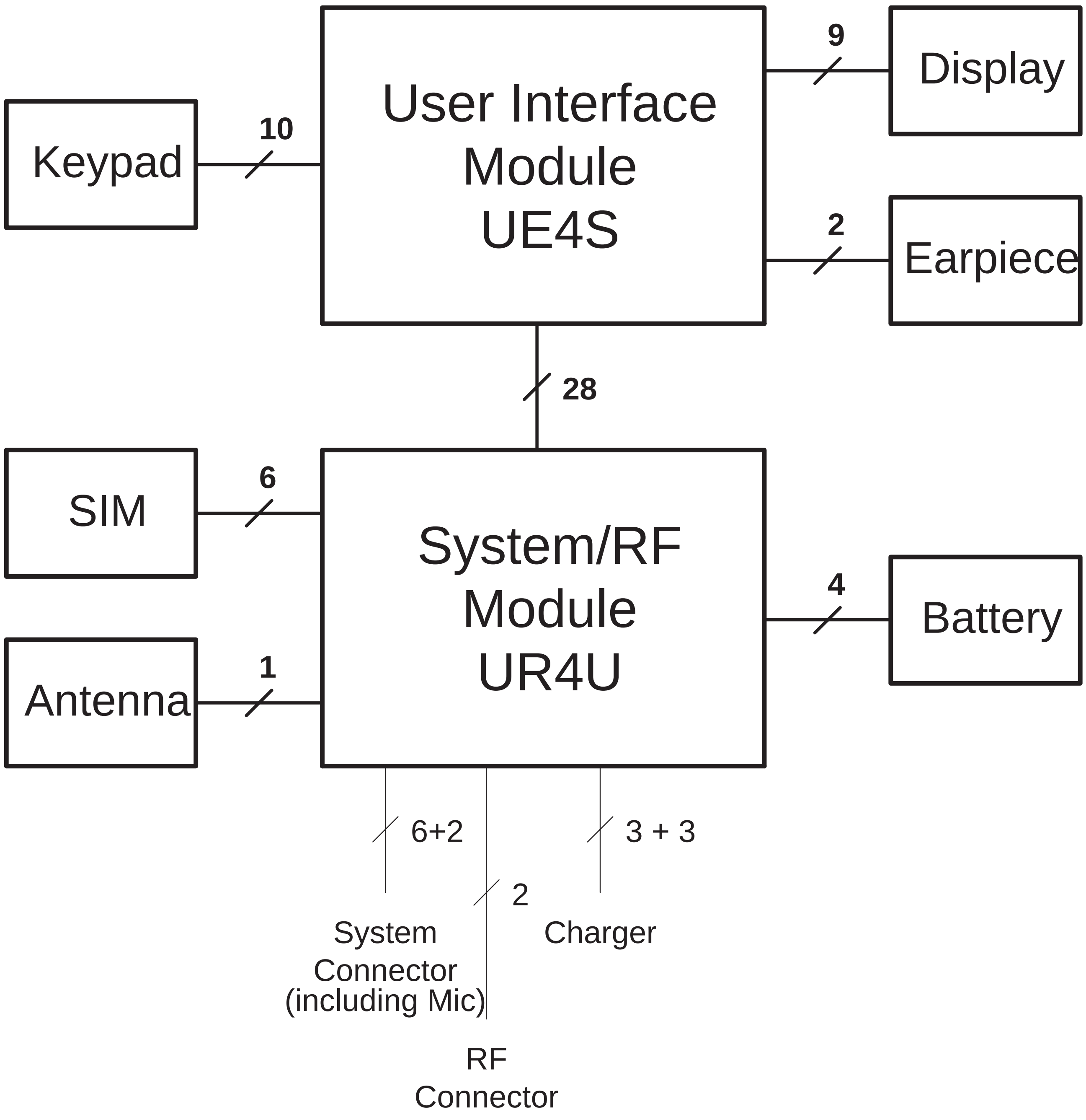
In the idle mode circuits are powered down and only sleep clock is running.

In the active mode all the circuits are supplied with power although some parts might be in the idle state part of the time.

The charge mode is effective in parallel with all previous modes. The charge mode itself consists of two different states, i.e. the charge and the maintenance mode.

The local mode is used for alignment and testing.

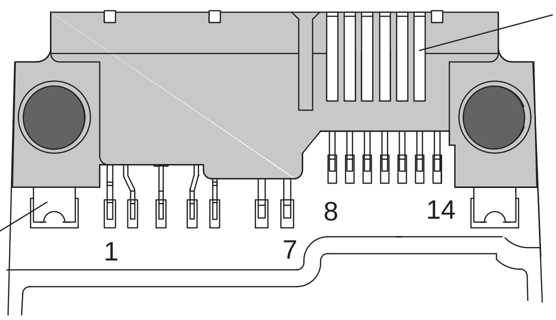
Interconnection Diagram

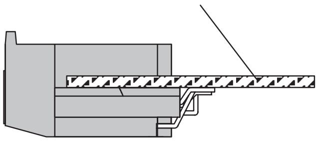


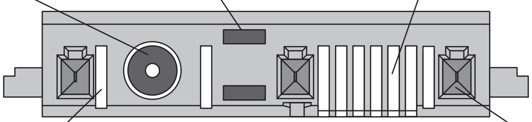
System Module

External and Internal Connectors

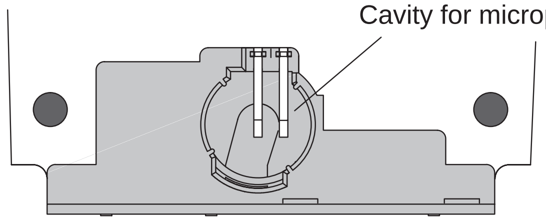
B side view







A side view

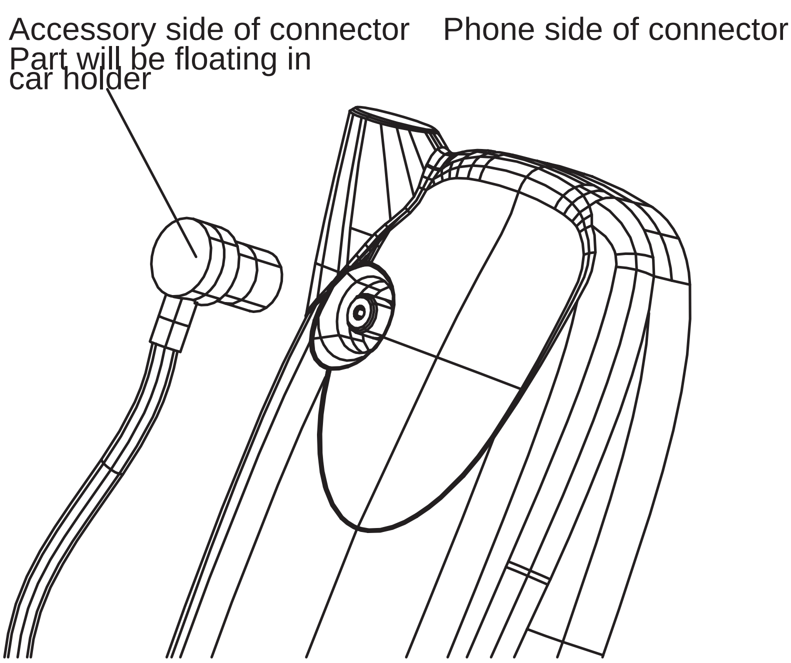


System Connector Signals

Pin	Name	Function	Description
1	V_IN	Bottom charger contacts	Charging voltage.
2	L_GND	DC Jack	Logic and charging ground.
3	V_IN	DC Jack	Charging voltage.
4	CHRG_CTRL	DC Jack	Charger control.
5	CHRG_CTRL	Bottom charger contacts	Charger control.
6	MICP	Microphone	Microphone signal, positive node.
7	MICN	Microphone	Microphone signal, negative node.
8	XMIC	Bottom & IBI connectors	Analog audio input.
9	SGND	Bottom & IBI connectors	Audio signal ground.
10	XEAR	Bottom & IBI connectors	Analog audio output.
11	MBUS	Bottom & IBI connectors	Bidirectional serial bus.
12	FBUS_RX	Bottom & IBI connectors	Serial data in.
13	FBUS_TX	Bottom & IBI connectors	Serial data out.
14	L_GND	Bottom charger contacts	Logic and charging ground.

RF–Connector

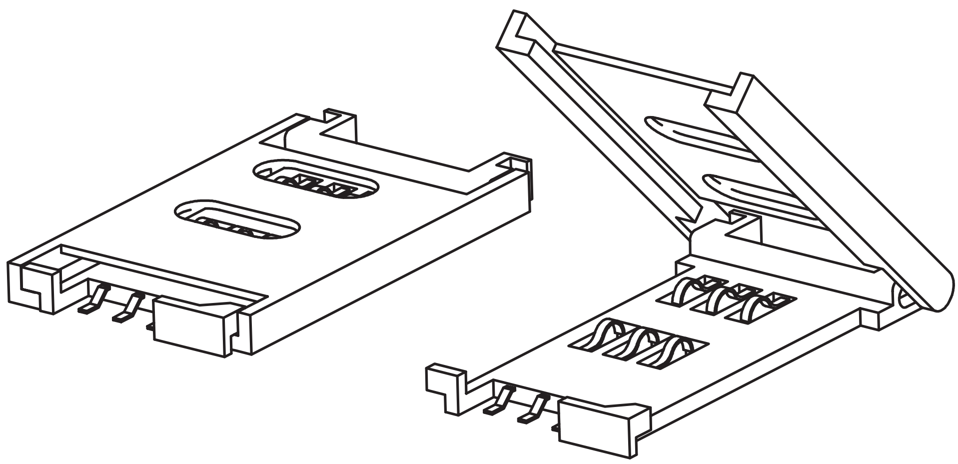
The RF–connector is needed to utilize the external antenna with Car Cradle. The RF–connector is located on the back side of the transceiver on the top section. The connector is plug type connector with special mechanical switching.



Battery Contacts

Pin	Name	Function	Description
1	BVOLT	Battery voltage	Battery voltage
2	BSI	Battery Size Indicator	Input voltage
3	BTEMP	Battery temperature indication Phone power up Battery power up PWM to VIBRA BATTERY	Input voltage Input voltage Output voltage PWM output signal frequency
4	BGND		Ground

SIM Reader



Operating Conditions

Environmental condition	Ambient temperature	Notes
Normal operation conditions	+7 ^{o}C ... +40 ^{o}C	Specifications fulfilled and fast charging possible
Extreme operation conditions	–10 ^{o}C ... +55 ^{o}C	Specifications fulfilled
Reduced performance conditions	+55 ^{o}C ... +65 ^{o}C	Operational only for short periods
Intermittent operation conditions	–25 ^{o}C ... –10 ^{o}C and +65 ^{o}C ... +80 ^{o}C	Operation maybe not possible but attempt to operate will not damage the phone
Cessation of operation	<–25 ^{o}C and >80 ^{o}C	No storage or operation attempt possible without permanent dam– age
Long term storage conditions	0 ^{o}C ... +40 ^{o}C	Battery only up to +30 ^{o}C !
Short term storage, max. 96 h	–25 ^{o}C ... +70 ^{o}C	Cumulative for life–time of battery

Environmental condition	Ambient temperature	Notes
Short term storage, max. 12 h	–25 ^{o}C ... +80 ^{o}C	Cumulative for life–time of battery
	–25 ^{o}C ... +75 ^{o}C	LCD operation
Short term operation	> +70 ^{o}C	Maximum value for SIM card, GSM spec. 11.11

Functional Description

The DCS 1900 engine consist of a Baseband/RF module with connections to a separate user interface module. Baseband and RF modules are interconnected with PCB wiring. The engine can be connected to accessories via the bottom system connector, the Intelligent Battery Interface (IBI) connector.

The RF submodule receives and demodulates radio frequency signals from the base station and transmits modulated RF signals to the base station. It consists of functional submodules Receiver, Frequency Synthesizer and Transmitter.

The Baseband module comprises audio, control, signal processing and power supply functions. It consists of functional submodules CTRLU (Control Unit; MCU, DSP, logic and memories), PWRU (Power Supply; regulators and charging) and AUDIO_RF (audio coding, RF–BB interface).

Modes of Operation

UR4 operates in cellular mode and a local mode for service:

– Cellular mode, phone controlled by OS and partly by base station
– Locals mode, used by Production and After Sales.
– Acting Dead mode
– Power Off mode
– Flash mode

Cellular Mode

In cellular mode phone performs all the tasks to place and release calls. Also charging and communication between accessories and phone are done during this mode by OS. Signaling and handover functions are supported by base station.

Power off

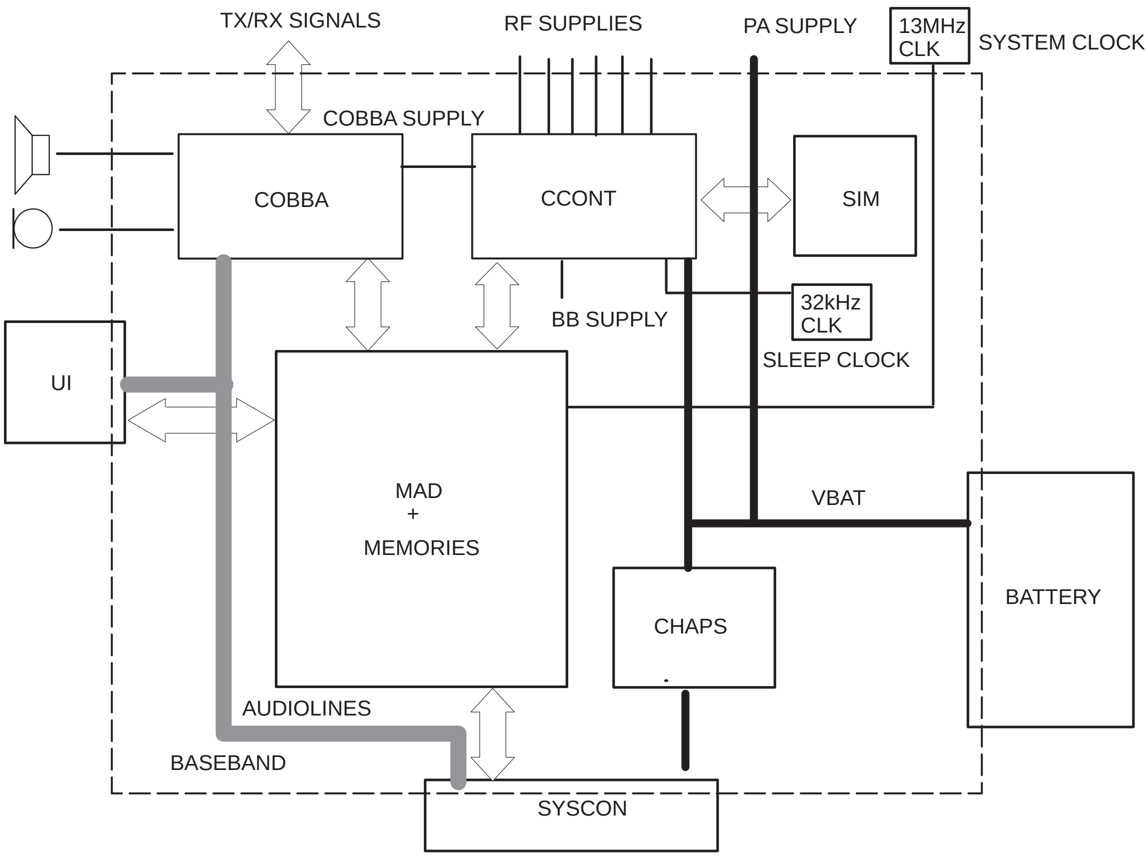
In the power–off mode only CCONT is active. Power–off mode can be left by pushing the PWR–key, connecting charger to the phone, real time clock interrupt or intelligent battery interrupt.

Locals Mode

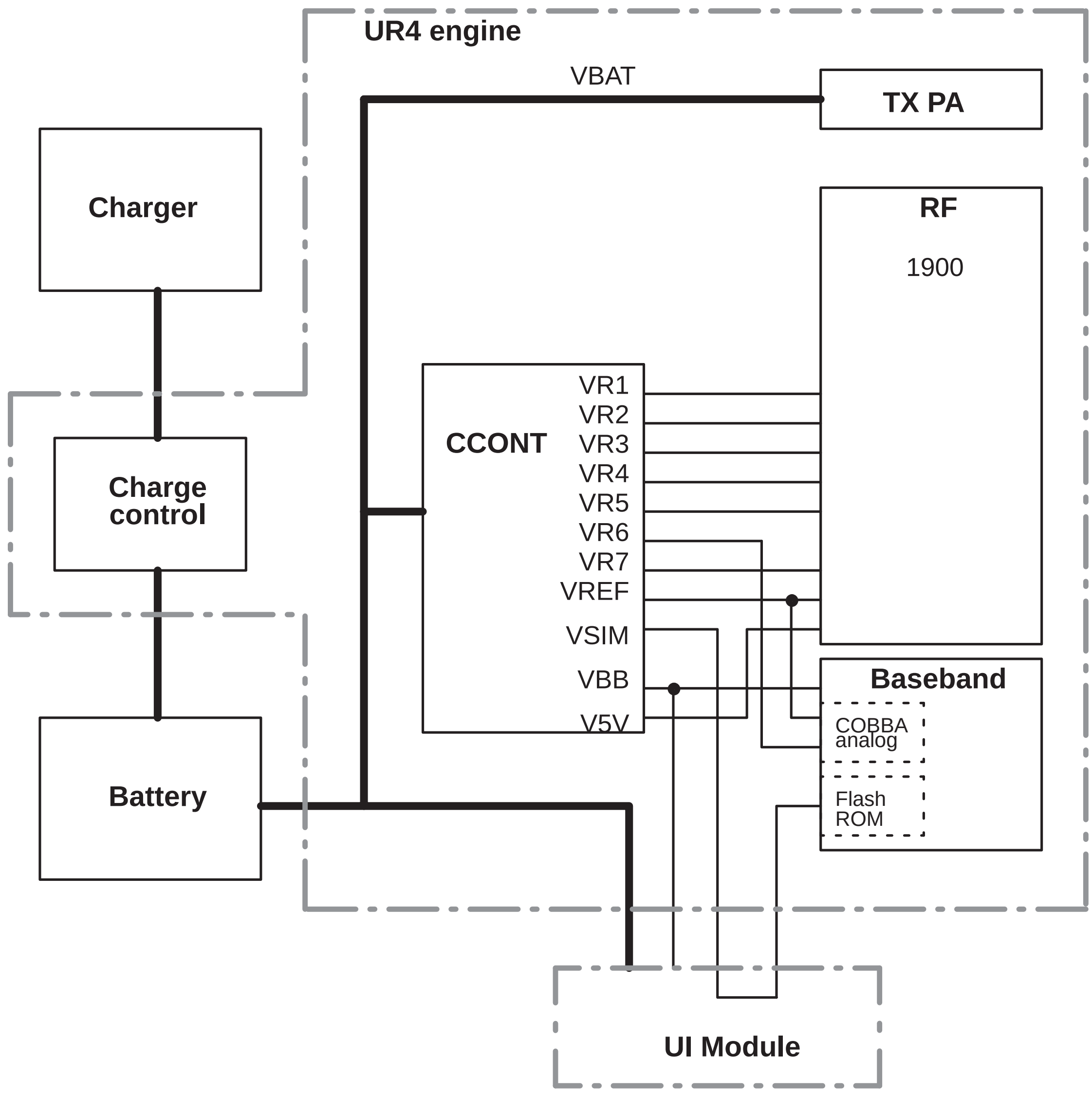
Locals mode is used for testing purposes by Product Development, Production and After Sales. The Cellular Software is stopped (no signalling to base station), and the phone is controlled by MBUS/FBUS messages by the controlling PC.

Baseband Module

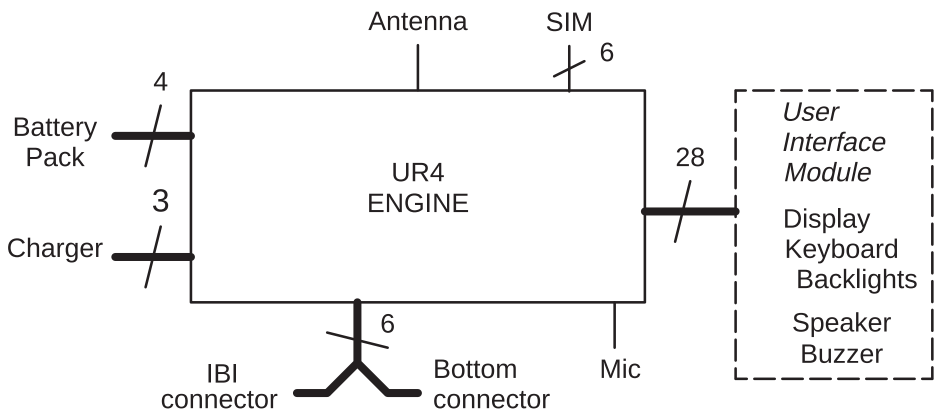
Block Diagram



Power Distribution Diagram



External interfaces



Connector Name	Code	Notes
Bottom & IBI connector	5469061	Includes DC plug, external audio, and data lines.
User Interface Module connector	5460021	28 pins, spring contacts.
Battery connector	5469069	2 pieces, 2 connections each.
SIM connector	5400085	Supports 3V/5V SIM cards.
RF connector	5429007	

Flash Programming connector

The system connector can be used as a flash prom programming interface for flash memories for updating (i.e. re–programming) the flash program memory.

The phone has to be switched off, when the flash prommer is connected to the phone system connector. The baseband is powered up as the supply voltage is connected to the charger contacts, or by pressing the PWR button, or by an IBI device..

The program execution starts from the BOOT ROM and the MCU investigates in the early start–up sequence if the flash prommer is connected. This is done by checking the status of the MBUS–line. Normally this line is high but when the flash prommer is connected the line is forced low by the prommer. The flash prommer serial data receive line is in receive mode waiting for an acknowledgement from the phone. The data transmit line from the baseband to the prommer is initially high. When the baseband has recognized the flash prommer, the TX–line is pulled low. This acknowledgement is used to start the data transfer of the first two bytes from the flash prommer to the baseband on the RX–line. The data transmission begins by starting the serial transmission clock (MBUS–line) at the prommer.

The 3V programming voltage is supplied inside the transceiver from the battery voltage with a switch mode regulator (3V/30mA) of the CCONT. The voltage is fed via UI connector to avoid damage of the CCONT during production line flashing (12V fed to FLASH Vpp from the production tester).

Pin	Name	Parameter	Min	Typ	Max	Unit	Remark
1	VIN	Charging	6.8	7.8	8.8	V	Supply Voltage,Current limited to 850 mA
11	MBUS	Serial clock from the Prommer	2.0 0		2.8 0.8	V	Prommer detection and Serial Clock for synchronous communication
12	FBUS_RX	Serial data from the Prommer	2.0 0		2.8 0.8	V	Receive Data from Prommer to Baseband
13	FBUS_TX	Data acknowledge to the Prommer	2.0 0		2.8 0.8	V	Transmit Data from Baseband to Prommer
14	GND	GND	0		0	V	Supply ground

Battery connector

The BSI contact on the battery connector is used to detect when the battery is to be removed to be able to shut down the operations of the SIM card before the power is lost if the battery is removed with power on. The BSI contact in the battery pack should be shorter than the supply power contacts to give enough time for the SIM shut down.

A vibra alerting device is used for giving silent signal to the user of an incoming call. The device is not placed in the phone but it will be added to a special battery pack. The vibra is controlled with a PWM signal by the MAD via the BTEMP battery terminal.

SIM card connector

Pin	Name	Parameter	Min	Typ	Max	Unit	Notes
1	GND	GND	0		0	V	Ground
2	VSIM	5V SIM Card 3V SIM Card	4.8 2.8	5.0 3.0	5.2 3.2	V	Supply voltage
3	DATA	5V Vin/Vout 3V Vin/Vout 	4.0 0 2.8 0	”1” ”0” ”1” ”0”	VSIM 0.5 VSIM 0.5	V	SIM data Trise/Tfall max 1us
4	SIMRST	5V SIM Card 3V SIM Card	4.0 2.8	”1” ”1”	VSIM VSIM	V	SIM reset
5	SIMCLK	Frequency Trise/Tfall	1.625	3.25	5.0 25	MHz ns	SIM clock

Real time clock

Requirements for a real time clock implementation are a basic clock (hours and minutes), a calender and a timer with alarm and power on/off –function and miscellaneous calls. The RTC will contain only the time base and the alarm timer but all other functions (e.g. calendar) will be implemented with the MCU software. The RTC needs a power backup to keep the clock running when the phone battery is disconnected. The backup power is supplied from a rechargable polyacene battery that can keep the clock running some ten minutes. If the backup has expired, the RTC clock restarts after the main battery is connected. The CCONT keeps MCU in reset until the 32kHz source is settled (1s max).

The CCONT is an ideal place for an integrated real time clock as the asic already contains the power up/down functions and a sleep control with the 32kHz sleep clock, which is running always when the phone battery is connected. This sleep clock is used for a time source to a RTC block.

Signals between baseband and User Interface section

The User interface section is implemented on separate UI board, which connects to the engine board with a board to board spring connector.

User Interface module connection

The User interface section comprises the keyboard with keyboard lights, display module with display lights, an earphone and a buzzer.

Earphone

The internal earphone is connected to the UI board by means of mounting springs for automatic assembly. The low impedance, dynamic type earphone is connected to a differential output in the COBBA audio codec. The voltage level at each output is given as reference to ground. Earphone levels are given to 32 ohm load.

Buzzer

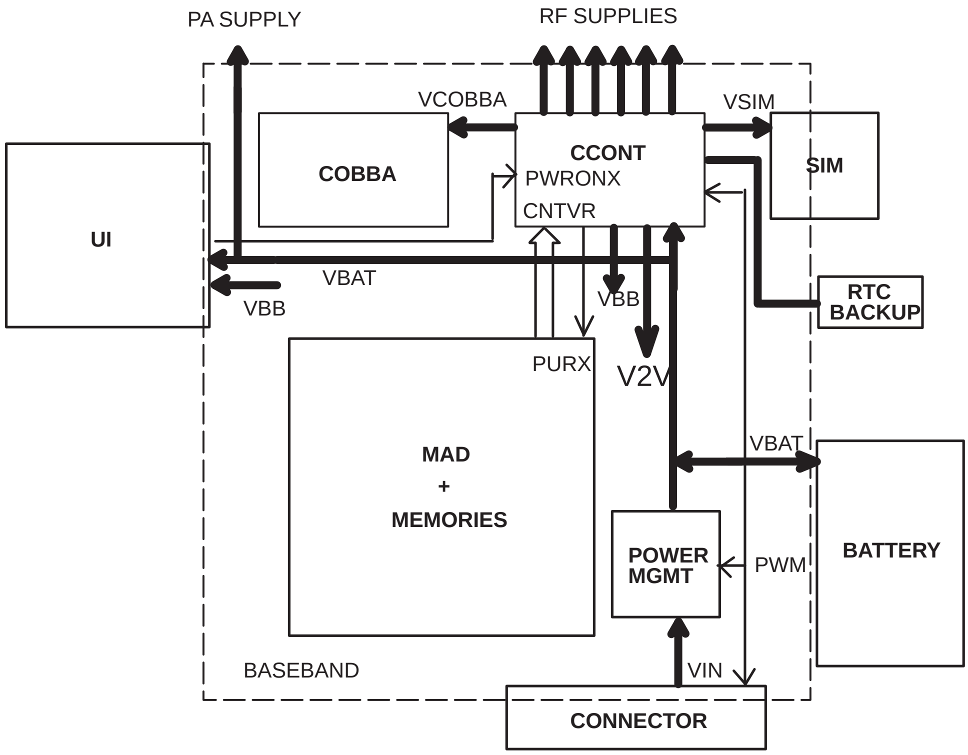
Alerting tones and/or melodies as a signal of an incoming call are generated with a buzzer that is controlled with a PWM signal by the MAD. Also key press and user function response beeps are generated with the buzzer. The buzzer is a SMT device and is placed on the UI board.

Power Distribution

In normal operation the baseband is powered from the phone‘s battery. The battery consists of one Lithium–cell. There is also a possibility to use batteries consisting of three Nickel–cells. An external charger can be used for recharging the battery and supplying power to the phone. The charger can be either so called fast charger, which can deliver supply current up to 850 mA or a standard charger that can deliver around 300 mA.

The baseband contains components that control power distribution to whole phone excluding the power amplifier, which have a continuous power rail direct from the battery. The battery feeds power directly to three parts of the system: CCONT, power amplifier, and UI (buzzer and display and keyboard lights).

The power management circuitry provides protection against overvoltages, charger failures and pirate chargers etc. that would otherwise cause damage to the phone. The circuitry is implemented in the beginning with discrete components, but it will be partly or fully integrated on later phase.



The heart of the power distribution is the CCONT. It includes all the voltage regulators and feeds the power to the whole system. The whole baseband is powered from the same regulator which provides 2.8V baseband supply VBB. The baseband regulator is active always when the phone is powered on. The baseband regulator feeds MAD and memories, COBBA digital parts and the LCD driver in the UI section. There is a separate regulator for a SIM card.

The regulator is selectable between 3V and 5V and controlled by the SIMPwr line from MAD to CCONT. SIM card regulator is also used for after sales flash programming. COBBA analog parts are powered from a dedicated 2.8V supply VCOBBA by the CCONT. The CCONT supplies also 5V for RF. The CCONT contains a real time clock function, which is powered from a RTC backup when the main battery is disconnected. The RTC backup is rechargeable polyacene battery.

CCONT includes also six additional 2.8V regulators providing power to the RF section. These regulators can be controlled either by the direct control signals from MAD or by the RF regulator control register in CCONT which MAD can update. Below are the listed the MAD control lines and the regulators they are controlling.

– TxPwr controls VTX regulator (VR7)
– RxPwr controls and VRX regulators (VR2 and VR5)
– SynthPwr controls VSYN_A and VSYN_D regulators (VR4 and VR3)
– VCXOPwr controls VXO and VCOBBA regulators (VR1 and VR6)

CCONT generates also a 1.5 V reference voltage VREF to COBBA, PLUSSA and CRFU. The VREF voltage is also used as a reference to some of the CCONT A/D converters.

In addition to the above mentioned signals MAD includes also TXP control signal which goes to PLUSSA power control block and to the power amplifier. The transmitter power control TXC is led from COBBA to PLUSSA.

Regulator	Max.current	Unit	Vout	Unit	Notes
VR1	25	mA	2.8	V	VVCXO
VR2	25	mA	2.8	V	VDET
VR3	50	mA	2.8	V	VSYN_D
VR4	90	mA	2.8	V	VSYN_A
VR5	80	mA	2.8	V	VRX
VR6	100	mA	2.8	V	COBBA
VR7	150	mA	2.8	V	VTX .Depends on exter nal BJT
V2V	50	mA	1.3 – 2.65	V	MAD core voltage, in 225mV steps (1.975V default)
VBB ON VBB SLEEP	125 1	mA mA	2.8 2.8	V	current limit 250mA current limit 5mA
VSIM	30	mA	3.0/ 5.0	V	VSIM output voltage selectable,Used also for flashing. (VPP)
V5V	30	mA	5.0	V	for RF

Power up

The baseband is powered up by:

1. Pressing the power key, that generates a PWRONX interrupt signal from the power key to the CCONT, which starts the power up procedure.
2. Connecting a charger to the phone. The CCONT recognizes the charger from the VCHAR voltage and starts the power up procedure.

   Before battery voltage voltage rises over 3.0 V Charging Logic gives an initial charge (with limited current) to the battery. After battery voltage reaches that voltage limit the power up procedure is as described in the previous chapters.
3. A RTC interrupt. If the real time clock is set to alarm and the phone is switched off, the RTC generates an interrupt signal, when the alarm is gone off. The RTC interrupt signal is connected to the PWRONX line to give a power on signal to the CCONT just like the power key.
4. A battery interrupt. Intelligent battery packs have a possibility to power up the phone. When the battery gives a short (10ms) voltage pulse through the BTEMP pin, the CCONT wakes up and starts the power on procedure.

When the CCONT is activated, it switches on the baseband supply voltage and generates a power up reset signal PURX to the MAD. When the PURX reset is released, the MAD releases the system reset ExtSysReset and the internal MCUResetX signals and starts the boot program execution. If booting is succeeded program execution continues from flash program memory. When the phone is powered up with an empty battery pack using the standard charger, the charger may not supply enough current for standard power–up procedure and the power–up must be delayed.

Acting Dead

If the phone is off when the charger is connected, the phone is powered on but enters a state called ”acting dead”. To the user the phone acts as if it was switched off. A battery charging alert is given and/or a battery charging indication on the display is shown to acknowledge the user that the battery is being charged.

Active Mode

In the active mode the phone is in normal operation, scanning for channels, listening to a base station, transmitting and processing information. All the CCONT regulators are operating. There are several substates in the active mode depending on if the phone is in burst reception, burst transmission, if DSP is working etc..

Sleep Mode

In the sleep mode all the regulators except the baseband VBB and the SIM card VSIM regulators are off. Sleep mode is activated by the MAD after MCU and DSP clocks have been switched off. The voltage regulators for the RF section are switched off and the VCXO power control, VCXOPwr is set low. In this state only the 32 kHz sleep clock oscillator in CCONT is running. The flash memory power down input is connected to the VCXO power control, so that the flash is deep powered down during sleep mode.

The sleep mode is exited either by the expiration of a sleep clock counter in the CCONT or by some external interrupt, generated by a charger connection, key press, headset connection etc. The MAD starts the wake up sequence and sets the VCXOPwr control high. After VCXO settling time other regulators and clocks are enabled for active mode.

If the battery pack is disconnect during the sleep mode, the CCONT should power down the SIM in the sleep mode as there is no time to wake up the MCU.

Charging

The power management circuitry controls the charging current delivered from the charger to the battery. Charging is controlled with a PWM input signal, generated by the CCONT. The PWM pulse width is controlled by the MAD and sent to the CCONT through a serial data bus. The battery voltage rise is limited to a specified level by turning the switch off. Charging current is passed through protection ASIC CHAPS and monitored by measuring the voltage drop across a 220mohm resistor.

2–wire charging

With 2–wire charging the charger provides constant output current, and the charging is controlled by PWMOUT signal from CCONT to Charging Logic. PWMOUT signal frequency is selected to be 1 Hz, and the charging switch in Charging Logic is pulsed on and off at this frequency. The final charged energy to battery is controlled by adjusting the PWMOUT signal pulse width.

Both the PWMOUT frequency selection and pulse width control are made MCU which writes these values to CCONT.

3–wire charging

With 3–wire charging the charger provides adjustable output current, and the charging is controlled by PWMOUT signal from CCONT to Charger, with the bottom connector signal. PWMOUT signal frequency is selected to be 32 Hz, and the charger output current is controlled by adjusting the PWMOUT signal pulse width. The charger switch in Charging Logic is constantly on in this case.

Power Off

The baseband is powered down by:

1. Pressing the power key, that is monitored by the MAD, which starts the power down procedure.
2. If the battery voltage is dropped below the operation limit, either by not charging it or by removing the battery.
3. Letting the CCONT watchdog expire, which switches off all CCONT regulators and the phone is powered down.
4. Setting the real time clock to power off the phone by a timer. The RTC generates an interrupt signal, when the alarm is gone off. The RTC interrupt signal is connected to the PWRONX line to give a power off signal to the CCONT just like the power key.

The power down is controlled by the MAD. When the power key has been pressed long enough or the battery voltage is dropped below the limit the MCU initiates a power down procedure and disconnects the SIM power. Then the MCU outputs a system reset signal and resets the DSP. If there is no charger connected the MCU writes a short delay to CCONT watchdog and resets itself. After the set delay the CCONT watchdog expires, which activates the PURX and all regulators are switched off and the phone is powered down by the CCONT.

If a charger is connected when the power key is pressed the phone enters into the acting dead mode.

Audio control

The audio control and processing is taken care by the COBBA, which contains the audio and rf codecs, and the MAD, which contains the MCU, ASIC and DSP blocks handling and processing the audio signals.

Microphone and Earphone

The baseband supports three microphone inputs and two earphone outputs. The inputs can be taken from an internal microphone, a headset microphone or from an external microphone signal source. The microphone signals from different sources are connected to separate inputs at the COBBA asic. Inputs for the microphone signals are differential type.

The output for the internal earphone is a dual ended type output capable of driving a dynamic type speaker. The output for the external accessory and the headset is single ended with a dedicated signal ground SGND. Input and output signal source selection and gain control is performed inside the COBBA asic according to control messages from the MAD. Keypad tones, DTMF, and other audio tones are generated and encoded by the MAD and transmitted to the COBBA for decoding.

Speech processing

The speech coding functions are performed by the DSP in the MAD and the coded speech blocks are transferred to the COBBA for digital to analog conversion, down link direction. In the up link direction the PCM coded speech blocks are read from the COBBA by the DSP.

There are two separate interfaces between MAD and COBBA: a parallel bus and a serial bus. The parallel bus has 12 data bits, 4 address bits, read and write strobes and a data available strobe. The parallel interface is used to transfer all the COBBA control information (both the RFI part and the audio part) and the transmit and receive samples. The serial interface between MAD and COBBa includes transmit and receive data, clock and frame synchronization signals. It is used to transfer the PCM samples. The frame synchronization frequency is 8 kHz which indicates the rate of the PCM samples and the clock frequency is 1 MHz. COBBA is generating both clocks.

Alert Signal Generation

A buzzer is used for giving alerting tones and/or melodies as a signal of an incoming call. Also key press and user function response beeps are generated with the buzzer. The buzzer is controlled with a BuzzerPWM output signal from the MAD. A dynamic type of buzzer must be used since the supply voltage available can not produce the required sound pressure for a piezo type buzzer. The low impedance buzzer is connected to an output transistor that gets drive current from the PWM output. The alert volume can be adjusted either by changing the pulse width causing the level to change or by changing the frequency to utilize the resonance frequency range of the buzzer.

A vibra alerting device is used for giving silent signal to the user of an incoming call. The device is controlled with a VibraPWM output signal from the MAD. The vibra alert can be adjusted either by changing the pulse width or by changing the pulse frequency. The vibra device is not inside the phone, but in a special vibra battery.

Digital control

MAD

The baseband functions are controlled by the MAD asic, which consists of a MCU, a system ASIC and a DSP. The DCS/PCN specific asic is named as MAD2. There are separate controller asics in TDMA and JDC named as MAD1 and MAD3. All the MAD asics contain the same core processors and similar building blocks, but differ from each other in system specific functions, pinout and package types.

MAD2 contains following building blocks:

- ARM RISC processor with both 16–bit instruction set (THUMB mode) and 32–bit instruction set (ARM mode)
- TMS320C542 DSP core with peripherals:
  - API (Arm Port Interface memory) for MCU–DSP communication, DSP code download, MCU interrupt handling vectors (in DSP RAM) and DSP booting
  - Serial port (connection to PCM)
  - Timer
  - DSP memory
- BUSC (BusController for controlling accesses from ARM to API, System Logic and MCU external memories, both 8– and 16–bit memories)
- System Logic
  - CTSI (Clock, Timing, Sleep and Interrupt control)
  - MCUIF (Interface to ARM via BUSC). Contains MCU BootROM
  - DSPIF (Interface to DSP)
  - MFI (Interface to COBBA AD/DA Converters)
  - CODER (Block encoding/decoding and A51&A52 ciphering)
  - AccIF(Accessory Interface)
  - SCU (Synthesizer Control Unit for controlling 2 separate synthesizer)
  - UIF (Keyboard interface, serial control interface for COBBA PCM Codec, LCD Driver and CCONT)
  - SIMI (SimCard interface with enhanced features)
  - PUP (Parallel IO, USART and PWM control unit for vibra and buzzer)

The MAD operates from a 13 MHz system clock, which is generated from the 13Mhz VCXO frequency. The MAD supplies a 6,5MHz or a 13MHz internal clock for the MCU and system logic blocks and a 13MHz clock for the DSP, where it is multiplied to 52 MHz DSP clock. The system clock can be stopped for a system sleep mode by disabling the VCXO supply power from the CCONT regulator output. The CCONT provides a 32kHz sleep clock for internal use and to the MAD, which is used for the sleep mode timing. The sleep clock is active when there is a battery voltage available i.e. always when the battery is connected.

Memories

The MCU program code resides in an external program memory. MCU work (data) memory size is 512kbits. A serial EEPROM is used for storing the system and tuning parameters, user settings and selections, a scratch pad and a short code memory. The EEPROM size is 64kbits. The memory variation is managed using memory components with the same packages and pinouts for all memory sizes of the given types. The system parameters contain information of the used memories in that end product. The selected memory packages are TSOP48 for ROM, STSOP32 for RAM and SO8S for EEPROM .

The used flash memories are capable to perform erase and write operations with the supplied 3V programming voltage.

The BusController (BUSC) section in the MAD decodes the chip select signals for the external memory devices and the system logic. BUSC controls internal and external bus drivers and multiplexers connected to the MCU data bus. The MCU address space is divided into access areas with separate chip select signals. BUSC supports a programmable number of wait states for each memory range.

Program Memory

The MCU program code resides in the program memory. The program memory size is 8Mbits (512kx16) The default package is TSOP48.

The power down pin of FLASH is utilized in the system sleep mode by connecting the VCXOPwr to the flash power down pin to minimize the flash power consumption during the sleep.

SRAM Memory

The work memory size can vary depending on the product variation similarly to the program memory. The work memory is a static ram of size 512kbits (64kx8). The work memory is supplied from the common baseband VBB voltage and the memory contents are lost when the baseband voltage is switched off. All retainable data is stored into the EEPROM when the phone is powered down.

EEPROM Memory

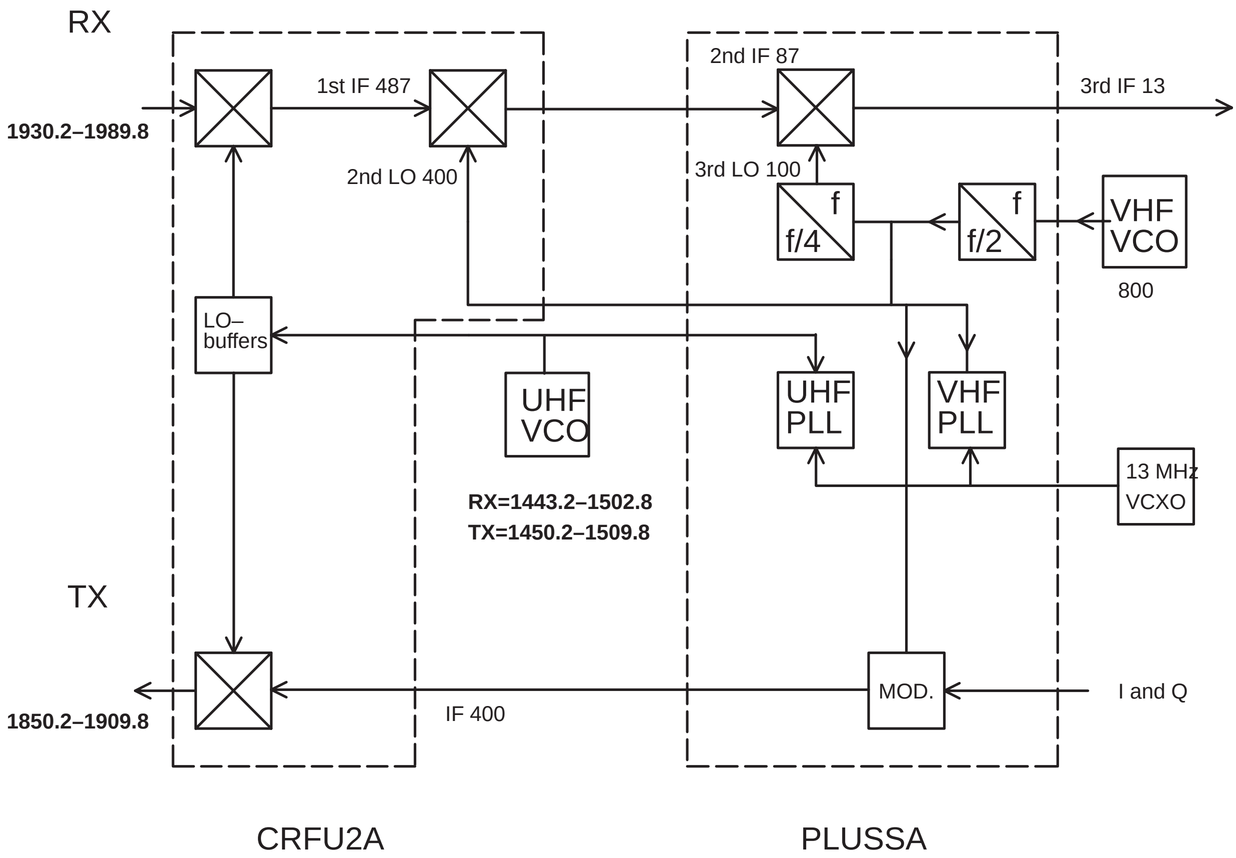
An EEPROM is used for a nonvolatile data memory to store the tuning parameters and phone setup information. The short code memory for storing user defined information is also implemented in the EEPROM. The EEPROM size is 8kbytes .The memory is accessed through a serial bus and the default package is SO8S.

MCU Memory Map

MAD supports maximum of 4GB internal and 4MB external address space. External memories use address lines MCUAd0 to MCUAd21 and 8–bit/16–bit data bus. The BUSC bus controller supports 8– and 16–bit access for byte, double byte, word and double word data. Access wait states (0, 1 or 2) and used data bus width can be selected separately for each memory block.

RF Module

RF Frequency Plan



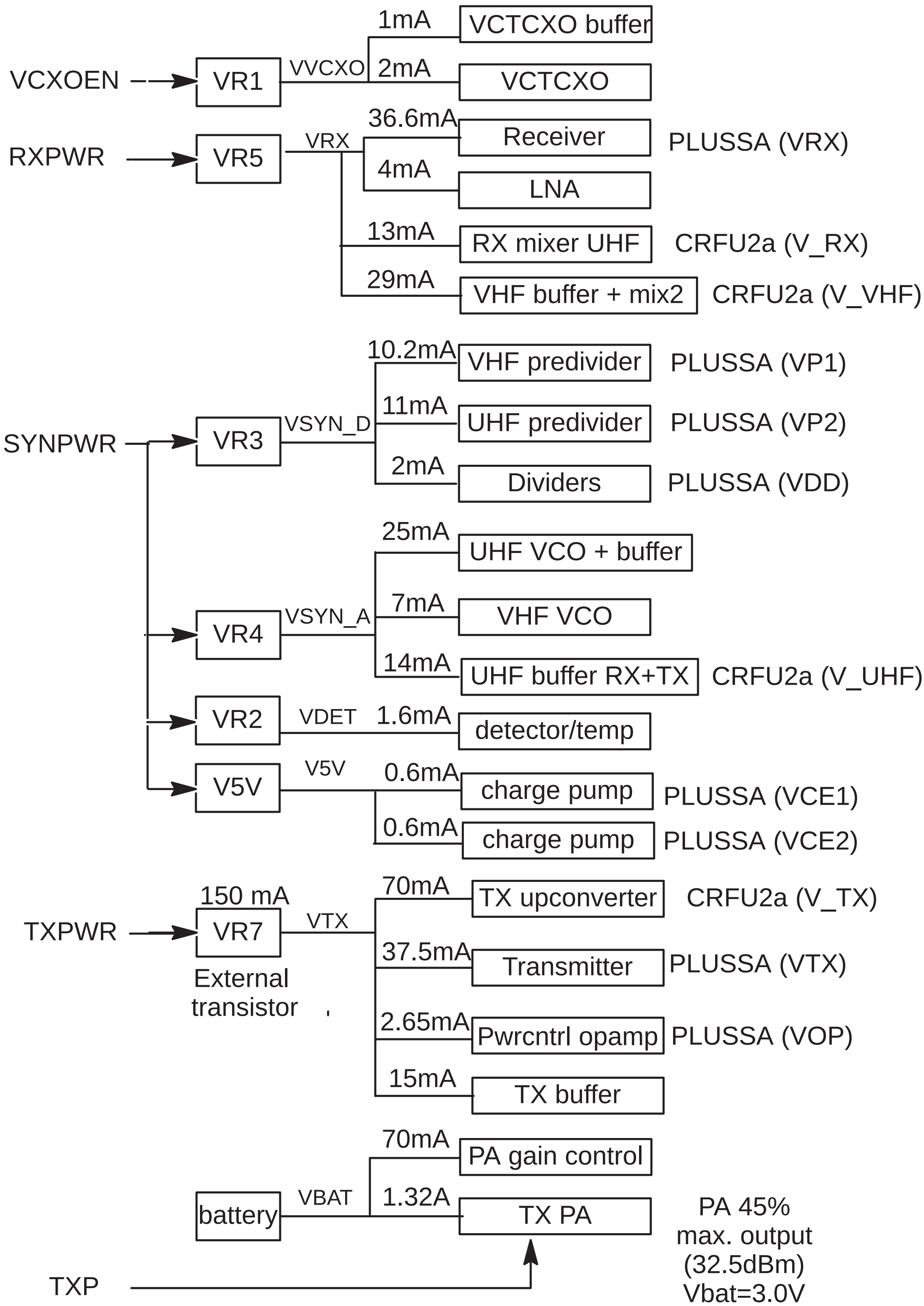
Note: 1 All frequencies are in MHz
2 Underlined frequencies are DCS1800
3 Bold frequencies are DCS1900
4 Other frequencies are common to both systems

DC Characteristics

Power Distribution Diagram

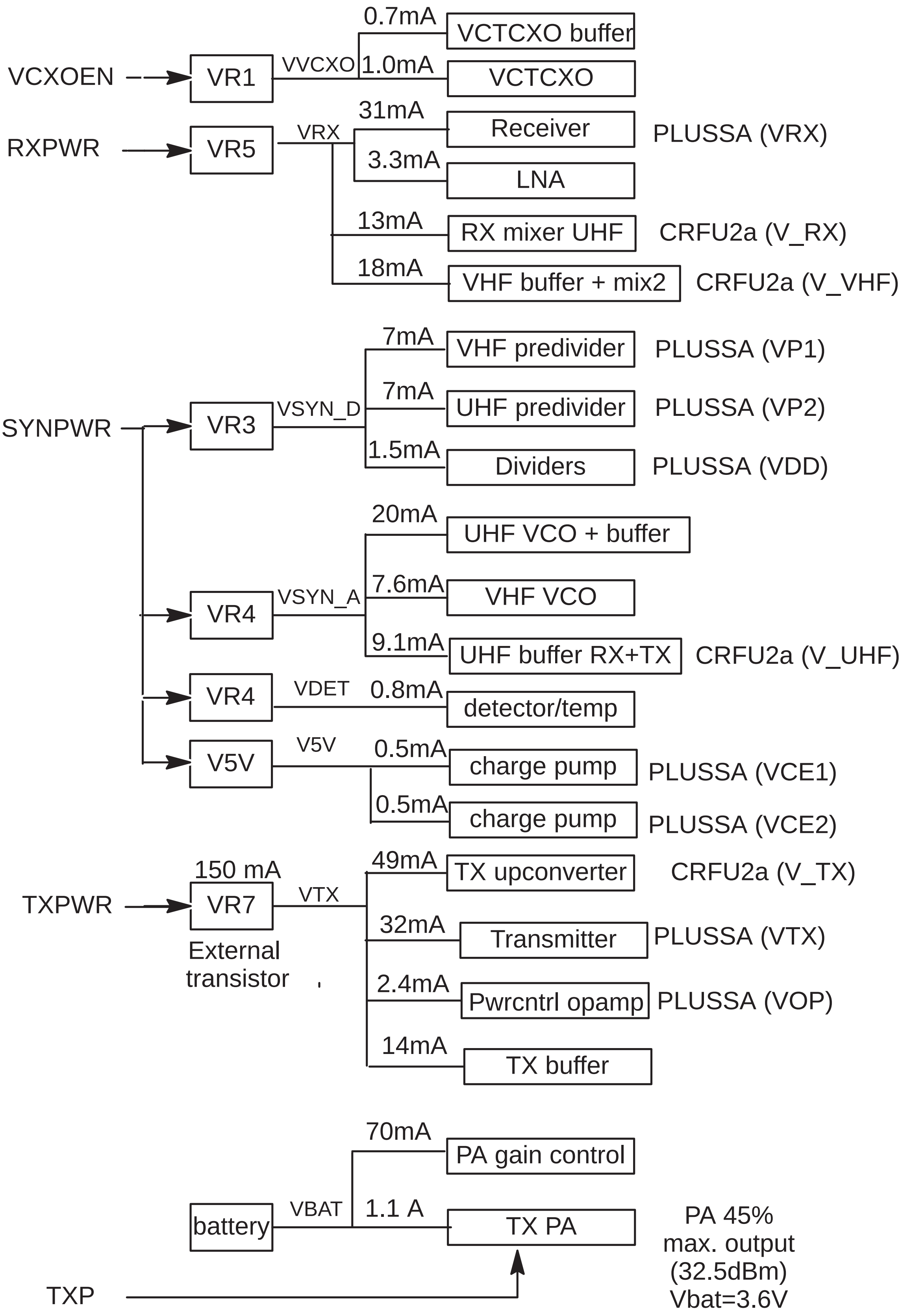
Current consumption of each regulator is shown in the following power distribution diagram (Figure 2 shows maximum currents, Figure 3 shows typical currents). On the left side of the figure, are the regulator control signals. Above each regulator is the rated current for that regulator. The name on the right side of the regulator block (smaller font) indicates the signal name used on the schematics. On the far right side of the figure are the pin names (power) for the different ICs.

Power Distribution – Maximum Currents



NOTE: Currents are only estimates at this time

Power Distribution – Typical Currents



Functional Description

The following description of the RF is valid for both DCS1800 and DCS1900, the only difference between the two systems is:

1. antenna
2. duplexer (Z401)
3. RX and TX interstage filters (Z604 and Z503/Z505)
4. UHF VCO modules (G701)
5. matching networks (discrete components)
6. PA (N500)

Even though different components are used in the two engines, the footprints of the different components are the same. As can been seen from the RF block diagram, most of the functions have been integrated into three ASICs.

CRFU2a (N402) is a wideband UHF ASIC with both receiver and transmitter functions. The receiver functions include LNA bias and two downconversion mixers (Gilbert cell) with LO buffers. The LNA transistor is external to CRFU2a. The transmitter functions include an upconversion mixer (image rejection) with LO buffer. All inputs/outputs are wideband and require external matching networks for optimal performance.

PLUSSA (N401) provides two main functions:

1. RX/TX blocks
2. PLL

The receiver includes a Receive Controlled Gain Amplifier, a mixer with LO buffers and IF amplifiers. The transmitter section includes a Transmit Controlled Gain Amplifier, an I/Q Modulator, circuitry required to generate the Quadrature Local Oscillator and Transmit Power Control which controls the MMIC PA (N500) output power. The PLL section is control via a serial bus and contains both UHF and VHF PLL and predividers.

The MMIC PA (N500) uses Ga–As– heterojunction bipolar transistor (GaAs HBT) technology. The PA has an overall dynamic range of 45dB, and is capable of producing 32.5dBm output power with +3dBm input.

Interfacing with the above ASICs is four more ASICs. These include:

1. CCONT (N100)– is a multifunction power management IC. This ASIC contains six 2.8V linear regulators used in the RF section as well as two 2.8V regulators used in the BB section. CCONT also contains a switch mode supply power which generates +5V which is used to power the charge pumps in PLUSSA. Some of the features of this IC are a nine channel A/D converter, power up/down procedures, reset logic, charging control, watchdog, sleep control and SIM interface.

2. COBBA_GJ (N300)– is an interface between the digital world of the BB processing and the analog world of RF and audio circuitry.

3. MAD2 (D200) – contains system logic and DSP

4. CHAPS (N110) – charging control ASIC

Receiver

The receiver is a triple conversion receiver consisting of two ASICs; CRFU2a (N402) and PLUSSA (N401). CRFU2a contains LNA bias circuitry with an external transistor which provides step gain depending on the incoming RF level and the first and second mixers. PLUSSA contains the third mixer. All filtering is external.

The received RF signal from the antenna is fed via the duplex filter (3 pole bandpass filter; Z401) to the LNA. Biasing and the AGC step circuitry are integrated into CRFU2a but the RF transistor, input and output matching networks are external. The LNA gain step is controlled by MAD2 (FRAC, D200). Gain step in LNA is activated when the receive RF level is below –48 dBm. Following the LNA, the signal is fed to a 3 pole ceramic bandpass filter (Z604). The combination of the duplex filter and the bandpass filter define, the blocking characteristics of the receiver.

The bandpass filtered signal is fed back to CRFU2a, where the signal is down converted with a double balanced active mixer (Gilbert cell) to 487 MHz. The local oscillator signal for this down conversion is generated by the UHF VCO (G701) and buffered in CRFU2a. The first IF signal is bandpass filtered with an 487 MHz SAW filter 7621. This filter attenuates the intermodulating and image frequencies. The second down conversion (occurs in CRFU2a) results in a balanced IF of 87 MHz which is filtered using an 87 MHz SAW filter (Z605). This filter provides selectivity for channels greater than +/– 200 kHz, and attenuates the image frequency of the third mixer and intermodulating signals. The local oscillator signal for this down conversion is 400 MHz which is generated by the 800 MHz VHF VCO module (G702). The VHF VCO signal is buffered and divided in PLUSSA and the 400 MHz resulting signal is again buffered in CFRU2a before the mixer.

After the 87 MHz filter, the signal is fed into the AGC amplifier which has been integrated into PLUSSA. The AGC amplifier contains analog gain control which provides accurate gain control (minimum 57 dB) for the receiver. Control voltage for the AGC is generated by the D/A–converter in COBBA_GJ (N300). The final mixing stage occurs in PLUSSA with a local oscillator signal of 100 MHz generated by dividing the VHF–synthesizer output (800 MHz) by eight.

The third (final) IF filter (Z606) is a ceramic bandpass filter with a centre frequency of 13 MHz. This filter attenuates adjacent channels with very little attenuation for +/– 200 kHz. The +/– 200 kHz interferers are filtered digitally by DSP. The 13 MHz bandpass signal is converted to a balanced signal with a buffer circuit in PLUSSA. This buffer circuit has a voltage gain of 36 dB. This balanced signal is then fed to COBBA_GJ. The PGA stage in COBBA_GJ has a gain setting of either 0 dB or 9.5 dB which is controlled via the COBBA_GJ control bus. For HD950 the PGA gain will be set to 0dB.

Transmitter

Transmitter chain consists of IQ–modulator, upconversion mixer, TX filter, TX buffer and a power amplifier.

The differential I and Q signals are generated by COBBA_GJ and are filtered by an external RC network (R501, R504, C525 and C526, fc=200kHz) before being fed into the IQ modulator in PLUSSA (N401). The modulator generates a TX IF of 400 MHz which is derived from the VHF synthesizer output (divide by two). Inside PLUSSA the 400 MHz is amplified and then fed to an external filter before being up–converted in CRFU2a. The up–converter in CRFU2a is a double balanced image rejection mixer. The local oscillator signal for the upconversion is generated by the UHF synthesizer. Following CRFU2a is a TX SAW Z503 filter which attenuates the image frequency, LO leakage and wideband noise. After the bandpass filter is a buffer V510 with 12dB gain, then a 3 pole ceramic bandpass filter (Z505) to further suppress spurious from the up–converter.

After filtering, the signal goes to the final amplifier, which is a MMIC PA (N500) with an input impedance of 50 ohms. The MMIC contains three amplifier stages with interstage matching. The first amplifier stage is variable and is control by the TX power control circuity. An external driver is required to supply the necessary current to the TX power control circuitry. The PA has over 45 dB power gain and is capable of producing an output of 32.5 dBm with an input of +3 dBm. Harmonics generated by the non-linear PA (class AB) are attenuated with the output external matching network and the lowpass/bandstop filtering in the duplexer (Z401).

Power control circuitry consists of a directional coupler power detector and an error amplifier in PLUSSA. The directional coupler is situated between the duplex filter and the external RF connector. With this configuration, variations in the IL of the duplexer are compensated by the control loop. The directional coupler converts the forward going power with a certain ratio into a signal which is rectified by a Schottky diode and a filter to create a DC voltage. This DC voltage is fed to the error amplifier in PLUSSA

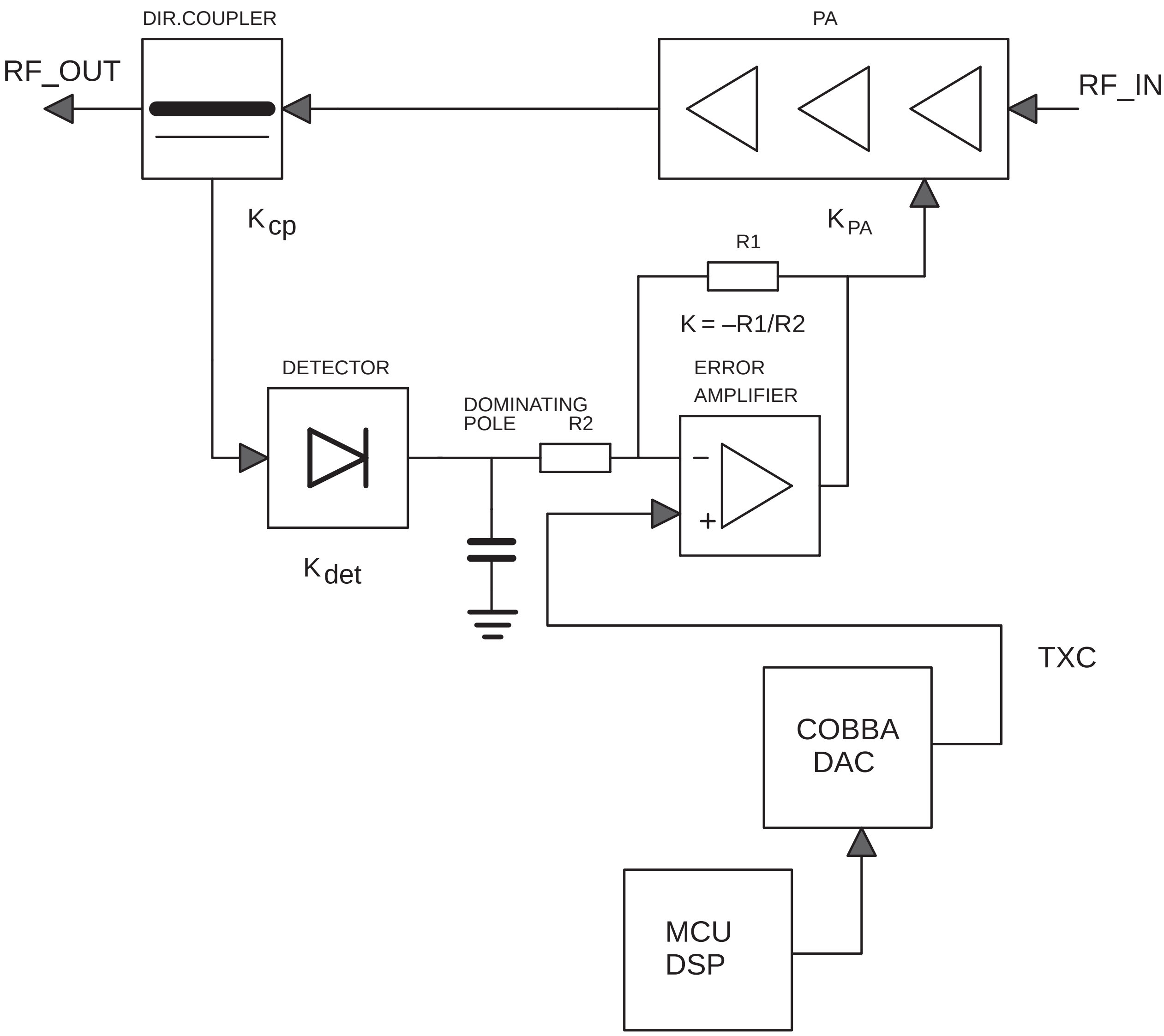
The error amplifier in PLUSSA compares the detected voltage and the TXC voltage, which is generated by a D/A converter in COBBA_GJ. This creates a closed control loop.

Power Detection Circuit

The power detector gives an indication of output RF power by rectifying the RF voltage to a DC voltage. Ideally the output voltage of this peak envelope detector is the peak value of the RF voltage but in real world the output voltage is somewhat smaller depending on the quality of the detector diode. Due to low supply voltage used in the phone the maximum envelope voltage of the detector is limited to about 1.5V. Over 30 dB power range this would yield a very low voltage at the lowest power level. The problem is circumvented by having a controllable attenuator limiting the detector input power at high power levels. A voltage doubling detector is being used to further increase the envelope voltage without need to increase the coupler coupling factor and antenna path losses excessively.

RF part of the power detector consists of schottky diode V501, bias resistors R531, 532, 502, capacitors C502, 535, 500, and 549. The bias voltage at diode output varies considerably with temperature. To eliminate this variation the detector output is coupled to the error amplifier through capacitor C520. Before transmission and between each burst the output end of the capacitor is connected to a stable reference potential with FET V506. The detector reference potential is formed from the regulated 2.8V supply with resistors R515 and 516. The FET is controlled according to VTX voltage by transistor V507. When VTX is down the FET is closed and C520 is charged with the potential difference between the detector bias potential and the detector reference voltage. Upon rise of VTX the FET is opened and the output end of C520 is allowed to follow the RF envelope voltage from the detector.

The detector reference voltage is about 0.5V. The bias voltage at the diode output is set 0.2 – 0.3V below the reference voltage at room temperature in order to avoid reverse voltage across tantalum capacitor C520 in cold temperature. A relatively large value of 4u7 was chosen for C520 for the case that the error amplifier gain would need to be limited with feedback resistors which would cause a current flowing through C520 changing the potential across it during the TX burst. A lower value will suffice if the error amplifier doesn't need current sourcing or sinking at the input.

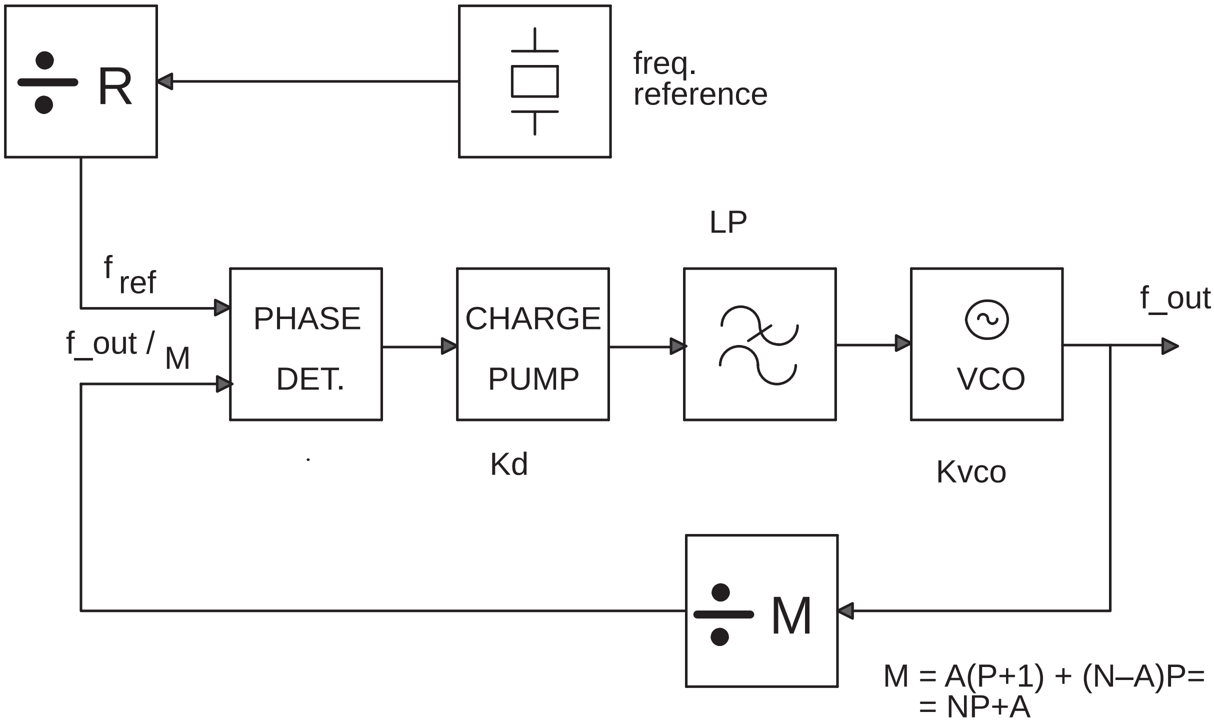

DIR.COUPLER
PA
RF_OUT
RF_IN
Kcp
KPA
R1
K = –R1/R2
DETECTOR
ERROR
AMPLIFIER
DOMINATING
POLE
R2
–
+
Kdet
TXC
COBBA
DAC
MCU
DSP

Frequency Synthesizers

A 13 MHz VCTCXO module is used as a stable reference for both the RF and BB circuitry. Temperature variations in the VCTCXO module are controlled by an AFC voltage which is generated by a 11 bit D/A converter in COB-BA_GJ. The output of the VCTCXO module feeds both the UHF PLL and the VHF PLL (both of which are located in PLUSSA) and the BB circuitry for A/D conversion. The BB uses this information for frequency compensation algorithms.

The UHF synthesizers contains a 64/65 dual modulus prescaler, a ”N” and ”A” divider, a reference divide, a phase detector, a charge pump, a modular VCO, a buffer circuit and a lowpass filter. The UHF and VHF PLL are controlled with three serial busses; a data bus (SDATA), a serial clock bus (SCLK) and a latch enable (SLE). The UHF LO signal is generated by the UHF VCO module which has a tunable frequency range from 1443 MHz to 1510 MHz for the DCS1900 engine. A sample of the LO signal is fed to the 64/65 prescaler. The signal is then fed to the programmable dividers (N and A) which are programmed via the serial bus. This output then becomes one of the inputs to the phase detector. The other input to the phase detector is a multiple of the 13MHz VCTCXO (reference frequency is 200 kHz). Output of the phase detector is connected to the charge pump, which charges or discharges the integrator capacitor in the loop filter depending on the phase of the measured frequency compared to reference frequency. The loop filter attenuates the pulses and generates a DC voltage which controls the frequency of UHF VCO. This loop filter defines the step response of the PLL (settling time), affects the stability of the loop and is used for sideband rejection. A buffer circuit is required to ensure that the impedance changes in CRFU2a and PLUSSA do not kick the VCO off frequency

The VHF synthesizers contains a 16/17 dual modulus prescaler, a ”N” and ”A” divider, a reference divide, a phase detector, a charge pump, a modular VCO and a lowpass filter. The frequency of the VHF VCO is 800 MHz which is frequency divided to 400 MHz and 100 MHz. Operation of the VHF PLL is similar to that of the UHF PLL. The VHF PLL using the 400 MHz signal as its input frequency. The reference frequency in the VHF synthesizer is 1 MHz.



AGC

The purpose of the AGC–amplifier is to maintain a constant output level from the receiver. The receiver is switched on approximately 150 μs before the burst begins, DSP measures the receive signal level and adjusts the TXC–DAC (which controls Receive Controlled Gain Amplifier) or it switches on/off the LNA with the FRAC control line. The Receive Controlled Gain Amplifier has 57 dB of continuos gain control (37 dB to –20 dB) while the gain in the LNA is a digital step and is either 15 dB or –24 dB.

The requirement for receive signal level (RSSI) under static conditions is that the MS shall measure and report to the BS over the range –48 dBm to –110 dBm. For RF levels above –48 dBm, the MS must report to BS the same reading, so above this level the AGC is not required. Because of the RSSI requirements, the gain step in LNA is ”ON” (FRAC = ”0”) for receive levels below –43 dBm. This leaves the AGC in PLUSSA to adjust the gain to desired value (50mVp–p). This is accomplished in DSP by measuring the receive IQ level after the selectivity filtering (IF–filters, ΣΔ±converter and FIR–filter in DSP). This results in an AGC dynamic range of 50 dB with the remaining 7 dB for gain variations in RX–chain (for calibration). For RF levels below –95 dBm, the output level of the receiver drops dB by dB with a level of 7.1 mVp–p @ –110 dBm for DCS1900.

This strategy is chosen because it is necessary to roll off the AGC in PLUSSA early so that the signal is not saturated in selectivity tests but cannot roll off too early as this will sacrifice the signal to noise ratio thus requiring a larger AGC dynamic range. The 50 mVp–p target level is set, because the RX–DAC in COBBA_GJ will saturate at 1.4 Vp–p. This results in over 28 dB of headroom which is required for the +/– 200 kHz faded adjacent channel (approximately 19 dB) and extra 9 dB for pre–monitoring.

AFC

The AFC is used to lock the MS clock to the frequency of the BS. An AFC voltage is generated in COBBA_GJ with an 11 bit ADC. This voltage then controls the center frequency of the 13 MHz VCTCXO module.

Software Compensations

Power Levels (TXC) vs. Channel

Power levels are calibrated on one channel in production. Values for channels between these tuned channels are calculated using linear interpolation.

Modulator Output Level

For optimum linearity and efficiency the output level of the modulator is adjusted in the production.

Power Levels vs temperature

In order to avoid the bias voltage variation of the detector diode ruining the accuracy of the power control loop, the bias voltage of the detector is measured when no RF power is transmitted. This voltage (DETLVL) is fed to the A/D converter in CCONT where DSP uses this value to correct the TXC voltage.

RSSI

Signal strength RSSI vs. input signal is calibrated in production, but RSSI vs. channel is compensated by software. If DETLVL (A/D) is used as a temperature sensor to correct for RX variations over temperature, the diode characteristics are 1.2mV/C.

RF Block Specifications

DCS1900 Receive Interstage Filter

Parameter	Min.	Typ.	Max.	Unit / notes
Passband	1930...1990			MHz
Insertion loss in passband			2.4	dB
Maximum Input power			1.0	W

First Mixer (UHF) in CRFU2a

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Input RF frequency	1805–1990			MHz
Output IF frequency		487		MHz
Power gain see Note 1	5.0		7.5	dB / PCN LO = 1318–1393 MHz
Power gain see Note 1	5.5		7.5	dB / DCS LO = 1443–1503 MHz
NF, SSB			11	dB
IIP3	–2			dBm
Input compression (1dB)	–10			dBm
1/2 IF spurious			tbd	dBm
LO–power in RF–input			–25	dBm
RF–IF isolation	20			dB

First IF Filter

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Center frequency		487		MHz
Input/Output impedance	in 240 Ω / –0.4 pF out 330 Ω / –0.2 pF			Ω
Ripple		0.5		dB
Insertion loss	2	2.5	4.5	dB
Attenuation @ 313 MHz	30			dB
Attenuation @ 400 MHz	30			dB

DCS1900 TX SAW filter

Parameter	Min.	Typ.	Max.	Unit / notes
Passband	1850 – 1910			MHz
Insertion loss in passband		3.2	4.2	dB

DCS1900 TX Ceramic Filter

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Passband	1850		1910	MHz
Insertion loss in passband			3.7	dB

Power Amplifier MMIC

Parameter	Symbol	Test condition	Min	Typ	Max	Unit
Operating freq. range		DCS1800 Application circuit	1710		1785	MHz
Operating freq. range		DCS1900 Application circuit	1850		1910	MHz
Supply voltage	Vcc		3.0	3.5	5.0	V
Gain control range (overall dynamic range)		Vpc= 0.5 ... 2.2 V	45			dB

Synthesizers Blocks

VHF VCO and Lowpass Filter

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Control voltage	0.5		4.0	V
Operation frequency		800		MHz
Output level	150			mVpp
Output impedance		50		Ω

UHF PLL

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Input frequency range ADDBIAS off	650		1300	MHz
Input frequency range ADDBIAS on	650		1700	MHz
Input signal level (f<1300MHz)	200			mVpp
Input signal level (f>1300MHz) ADDBIAS must be on	300			mVpp
Reference input frequency		13		MHz

DCS1900 UHF VCO module

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Control voltage (Vc)	0.8		3.7	V
Oscillation frequency	1443.2		1509.8	MHz
TX frequency range	1450.2		1509.8	MHz
RX frequency range	1443.2		1502.8	MHz
Tuning voltage at center frequency	2.0	2.25	2.5	V
Tuning voltage sensitivity	29	33	37	MHz/V
Output power level	–4.0			dBm

UHF LO signal into CRFU_2a

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Input frequency range PCN	1310		1395	MHz
Input frequency range DCS	1443		1510	MHz
Input level UHFLO_IN_P	–13 (140Ω)		–3 (261Ω)	dBm (measured input resistance)
Input level UHFLO_IN_M		N/A		This input is shorted to ground with a cap

Connections

RF connector and antenna switch

Parameter	Min.	Typ.	Max.	Unit/Notes
Operating frequency range	1710		1990	MHz
Nominal impedance		50		Ω
Insertion loss COM to INT			0.3	dB
Insertion loss COM to EXT			0.4	dB
Return loss, at COM port	15			dB
Power rating			2	W, 100% duty cycle
Contact resistance			25	mΩ
Insulation resistance (250VDC)	1000			MΩ

RF–Baseband signals

Signal name	From	To	Parameter	Mini-mum	Typi-cal	Maxi-mum	Unit	Func-tion
VBAT	Battery	RF	Voltage	3.0	3.6	5.0	V	Supply voltage for RF
VCXOEN	*MAD2*	*CCONT*	Logic high ”1”	2.0		VBAT	V	VR1, VRBB in CCONT ’ON’
			Logic low ”0”			0.5	V	VR1, VRBB in CCONT ’OFF’
			Input resistance	50	100	200	kΩ	
			Input capacitance			10	pF	
SYNPWR	*MAD2*	*CCONT*	Logic high ”1”	2.0		VBAT	V	VR3, VR4, V5, VR2 in CCONT ’ON’
			Logic low ”0”			0.5	V	
			Input resistance	50	100	200	kΩ	
			Input capacitance			10	pF	

Signal name	From	To	Parameter	Mini-mum	Typi-cal	Maxi-mum	Unit	Func-tion
RXPWR	*MAD2*	*CCONT*	Logic high ”1”	2.0		VBAT	V	VR5 in CCONT ’ON’
			Logic low ”0”			0.5	V	VR5 in CCONT ’OFF’
			Input resistance	50	100	200	kΩ	
			Input capacitance			10	pF	
TXPWR	*MAD2*	*CCONT*	Logic high ”1”	2.0		VBAT	V	VR7 in CCONT ’ON’
			Logic low ”0”			0.5	V	VR7 in CCONT ’OFF’
			Input resistance	50	100	200	kΩ	
			Input capacitance			10	pF	
VREF	CCONT	PLUSSA	Voltage	1.478	1.500	1.523	V	Reference voltage for PLUSSA
VVCXO	CCONT	VCTCXO	Voltage	2.7	2.8	2.85	V	VR1
VDET	CCONT	Detector circuit	Voltage	2.7	2.8	2.85	V	VR2
VSYN_D	CCONT	PLUSSA	Voltage	2.7	2.8	2.85	V	VR3
VSYN A	CCONT	VCOs CRFU	Voltage	2.7	2.8	2.85	V	VR4
VRX	CCONT	PLUSSA CRFU	Voltage	2.7	2.8	2.85	V	VR5
VTX	CCONT	PLUSSA CRFU	Voltage	2.7	2.7	2.85	V	VR7
V5V	CCONT	PLUSSA	Voltage	4.8	5.0	5.2	V	V5V, charge pump
FRAC	MAD2	CRFU2a	Logic high ”1”	2			V	Nominal gain in LNA
			Logic low ”0”			1	V	Reduced gain in LNA

Signal name	From	To	Parameter	Mini-mum	Typi-cal	Maxi-mum	Unit	Func-tion
SENA	MAD2	PLUSSA	Logic high ”1”	2.0			V	PLL enable
			Logic low ”0”	0		0.8	V	
SDATA	MAD2	PLUSSA	Logic high ”1”	2.0			V	Syn-thesiz-er data
			Logic low ”0”	0		0.8	V	
SCLK	MAD2	PLUSSA	Logic high ”1”	2.0			V	Syn-thesiz-er clock
			Logic low ”0”	0		0.8	V	
AFC	COBBA	VCXO	Output voltage swing	0	1.15	2.346	V	Auto-matic fre-quency control signal for VCXO
			Sampling rate		1	2	kHz	
			Minimum output voltage		0	0.046	V	
			Maximum output voltage	2.254	2.3	2.346	V	
RFCLK	VCTCXO	MAD2	Frequency		13		MHz	Stable clock signal for the logic circuits (clock slicer)
			Signal amplitude	0.5	1.0	2.0	Vpp	
RXP/RXN	PLUSSA	COBBA	Output level		0.05	1.4	Vpp	Differ-ential RX 13 MHz signal to base-band
TXIP/ TXIN	COBBA	PLUSSA	Number of bits		8		bits	Differ-ential in–phase TX base-band signal for the RF modu-lator
			Differential voltage swing (static)	1.022	1.1	1.18	Vpp	

Signal name	From	To	Parameter	Mini-mum	Typi-cal	Maxi-mum	Unit	Func-tion
TXQP/ TXQN	COBBA	PLUSSA	Same as TXIP/TXIN					Differ-ential quad-rature phase TX base-band signal for the RF modu-lator
TXP	MAD2	PLUSSA	Logic high ”1”	2.0			V	Trans-mitter power control enable
			Logic low ”0”			0.8	V	
TXC	COBBA	PLUSSA	Number of bits	10			bits	Trans-mitter power control
			DNL			±0.9	LSB	
			INL			±4	LSB	
			Output voltage swing	2.09	2.15	2.21	V	
			Minimum code output level	0.12	0.15	0.18	V	
			Maximum code output level	2.27	2.3	2.33	V	

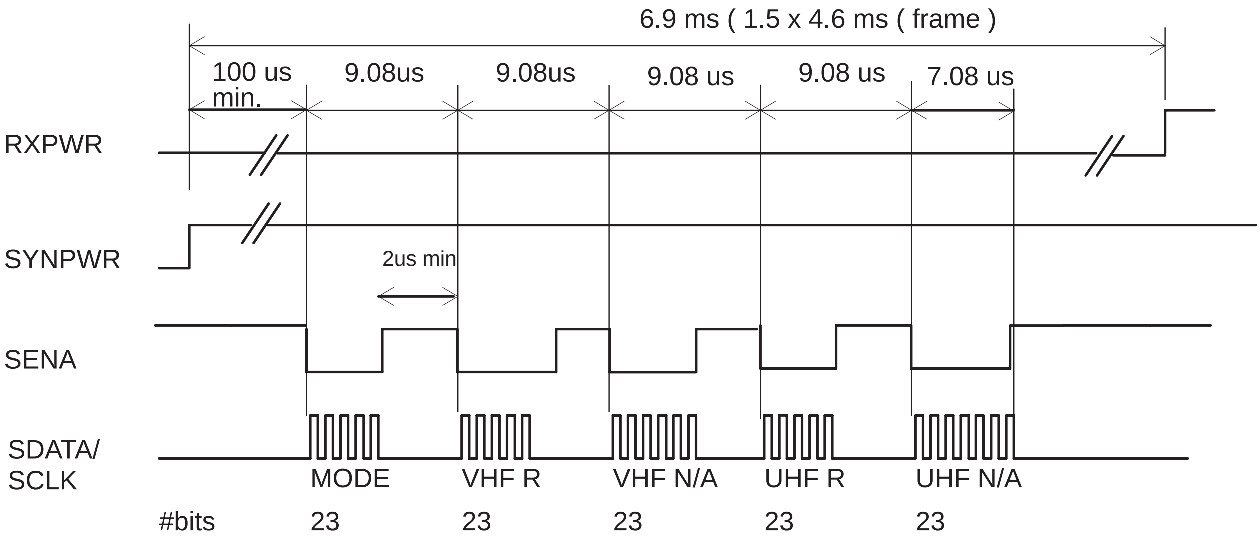
Signal name	From	To	Parameter	Mini-mum	Typi-cal	Maxi-mum	Unit	Func-tion
AGC	COBBA	PLUSSA	Number of bits	10			bits	Re-ceiver gain control
			DNL			±0.9	LSB	
			INL			±4	LSB	
			Output voltage swing	2.09	2.15	2.21	V	
			Minimum code out-put level	0.12	0.15	0.18	V	
			Maximum code out-put level	2.27	2.3	2.33	V	
DETLVL	Detector	CCONT pin 61 VCXO-TEMP	Input voltage	0.1		1.478	V	RSSI correc-tion
BASE_TUNE	Detector	CCONT pin 1 RSSI	Input voltage	0.1		1.478	V	Sam-ple of detec-tor out-put; DSP cor-rects TXC.

TXC and AGC signals originate from the same DAC, controlled in COBBA

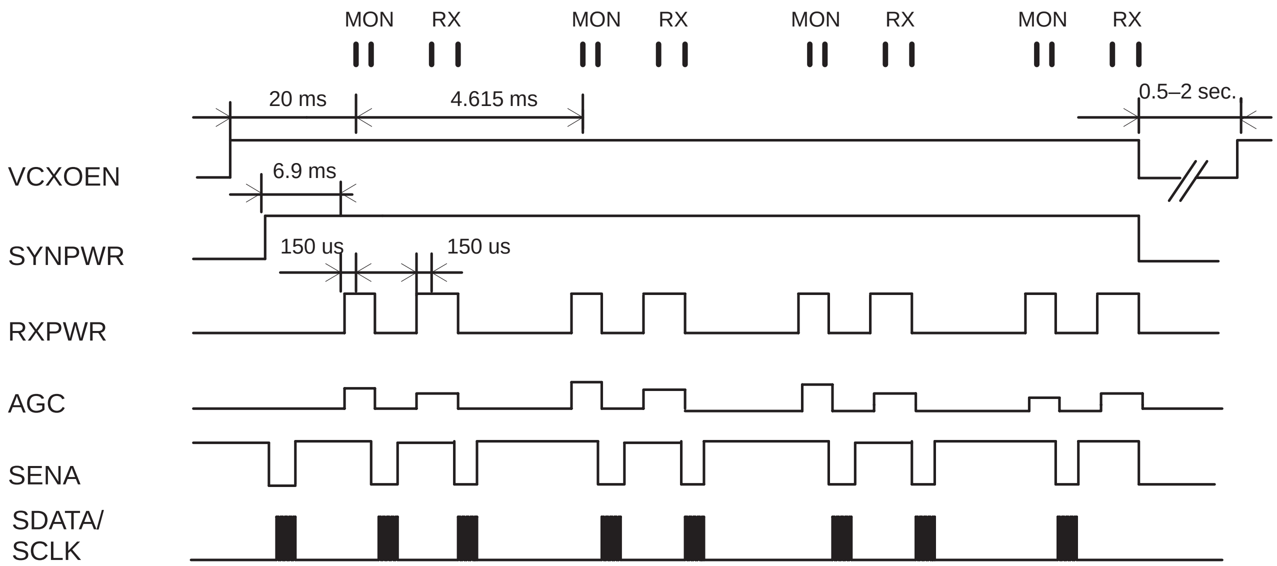
Data Interface and Timing

PLUSSA is programmed via the serial bus SLE, SDAT and SCLK. The data of SDAT is clocked by rising edge of SCLK. The data is fed MSB first and address bits before data bits. The data for the Programmable dual modulus counter is fed first and the Swallow counter last. SLE is kept low while clocking the data.
During programming, the charge pump attached to programmed divider is switched to high impedance state. Also all counters connected to the PLL that is programmed, are kept on reset while the SLE is low.

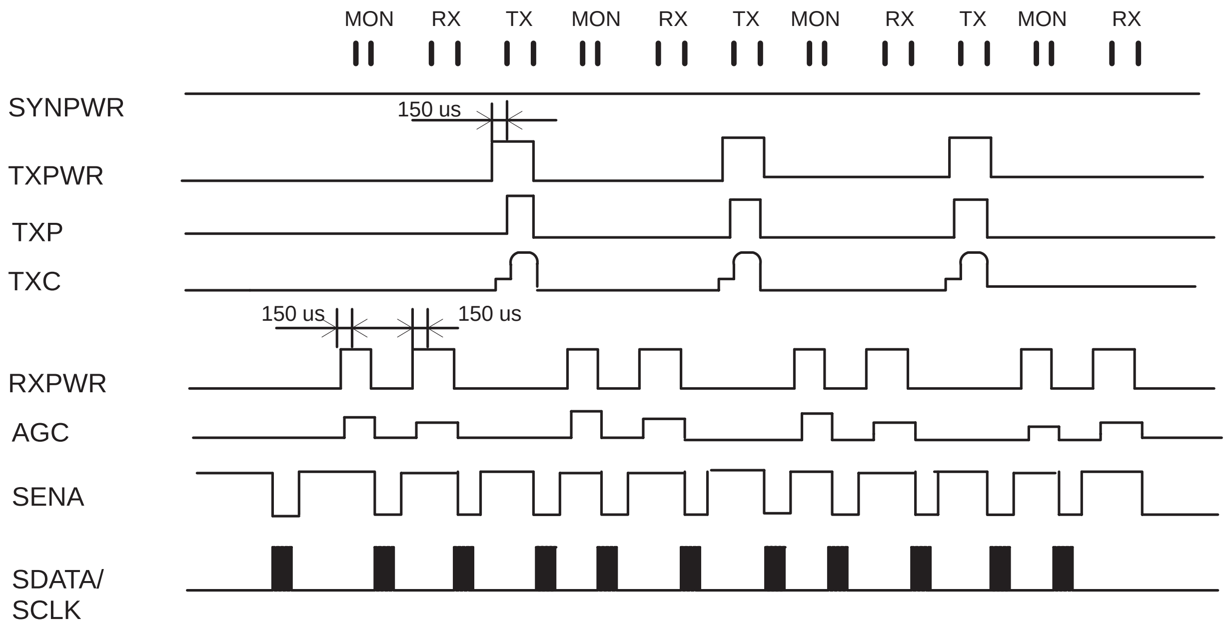
Synthesizer Timing Control



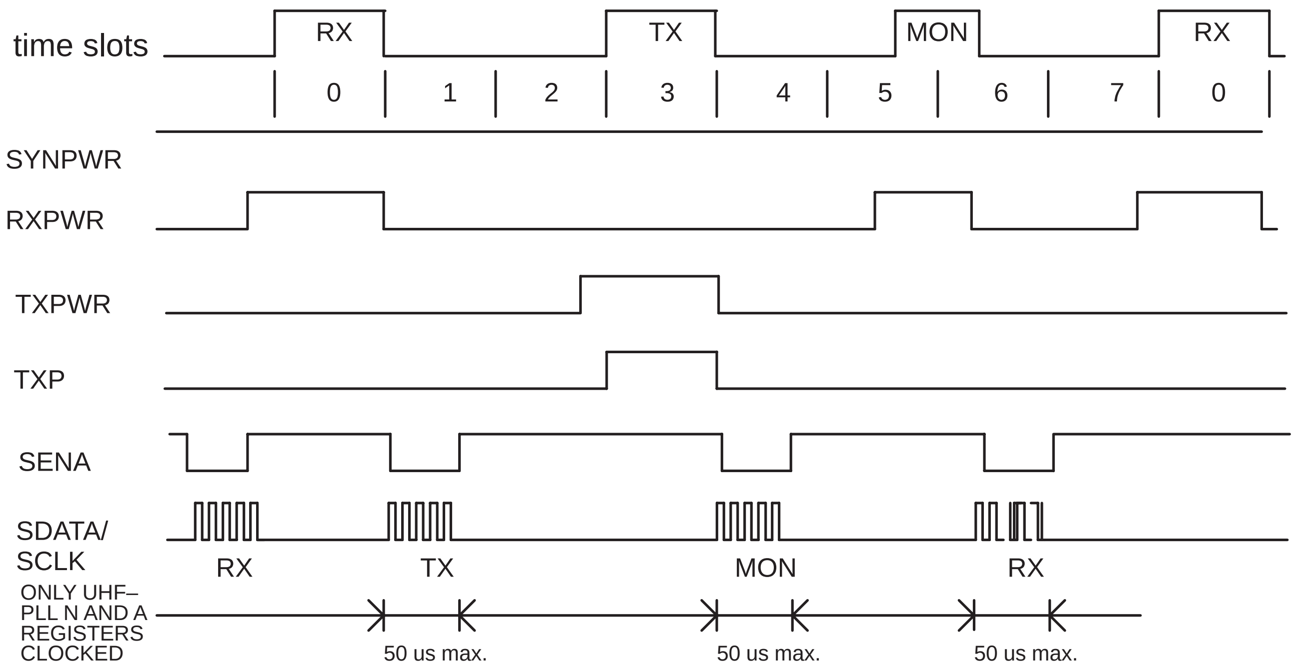
Synthesizer Start–up Timing / Clocking



Synthesizer Timing / IDLE one monitoring/frame,
frame can start from RX burst

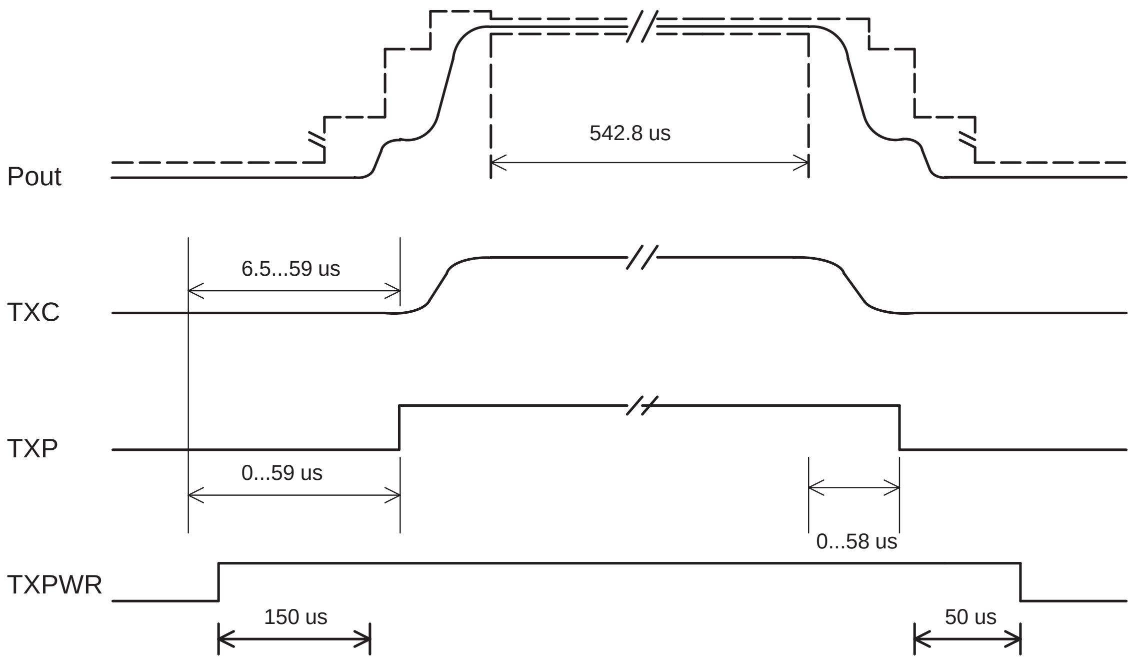


Synthesizer Timing / traffic channel



UHF–Synthesizer Timing / traffic channel

Transmit Power Timing



Transmitter Timing Diagram

Parts list of UR4U (EDMS Issue 16.4) Code: 0200962

ITEM	CODE	DESCRIPTION	VALUE	TYPE
R080	1620031	Res network 0w06 2x1k0 j	0404	0404
R081	1620031	Res network 0w06 2x1k0 j	0404	0404
R082	1620031	Res network 0w06 2x1k0 j	0404	0404
R083	1620031	Res network 0w06 2x1k0 j	0404	0404
R084	1620031	Res network 0w06 2x1k0 j	0404	0404
R087	1430690	Chip jumper		0402
R101	1620027	Res network 0w06 2x47r j	0404	0404
R103	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R104	1620025	Res network 0w06 2x100k j	0404	0404
R107	1620019	Res network 0w06 2x10k j	0404	0404
R109	1422881	Chip resistor	0.22	5 % 1 W 1218
R113	1620027	Res network 0w06 2x47r j	0404	0404
R117	1620101	Res network 0w06 2x470r j	0404	0404
R119	1430744	Chip resistor	470	5 % 0.063 W 0402
R123	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R125	1620027	Res network 0w06 2x47r j	0404	0404
R127	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R130	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R134	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R136	1825001	Chip varistor vwm18v vc40v	0603	0603
R137	1825001	Chip varistor vwm18v vc40v	0603	0603
R138	1825001	Chip varistor vwm18v vc40v	0603	0603
R139	1825001	Chip varistor vwm18v vc40v	0603	0603
R143	1620019	Res network 0w06 2x10k j	0404	0404
R144	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R146	1825005	Chip varistor vwm14v vc30v	0805	0805
R151	1825009	Varistor network 4xvwm18v	1206	1206
R153	1620031	Res network 0w06 2x1k0 j	0404	0404
R154	1430812	Chip resistor	220 k	5 % 0.063 W 0402
R155	1430812	Chip resistor	220 k	5 % 0.063 W 0402
R197	1430834	Chip resistor	3.3 M	5 % 0.063 W 0402
R198	1430826	Chip resistor	680 k	5 % 0.063 W 0402
R199	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R200	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R201	1430812	Chip resistor	220 k	5 % 0.063 W 0402
R202	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R207	1430690	Chip jumper		0402
R210	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R211	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R300	1620027	Res network 0w06 2x47r j	0404	0404
R301	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R302	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R308	1620025	Res network 0w06 2x100k j	0404	0404
R310	1430740	Chip resistor	330	5 % 0.063 W 0402
R332	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R333	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R334	1620031	Res network 0w06 2x1k0 j	0404	0404

R335	1430804	Chip resistor		100 k	5 % 0.063 W 0402
R338	1430718	Chip resistor		47	5 % 0.063 W 0402
R401	1430851	Chip resistor		15 k	2 % 0.063 W 0402
R501	1620019	Res network 0w06 2x10k j	0404		0404
R502	1430762	Chip resistor		2.2 k	5 % 0.063 W 0402
R503	1430740	Chip resistor		330	5 % 0.063 W 0402
R504	1620019	Res network 0w06 2x10k j	0404		0404
R505	1430804	Chip resistor		100 k	5 % 0.063 W 0402
R507	1430754	Chip resistor		1.0 k	5 % 0.063 W 0402
R508	1430804	Chip resistor		100 k	5 % 0.063 W 0402
R511	1430762	Chip resistor		2.2 k	5 % 0.063 W 0402
R512	1430778	Chip resistor		10 k	5 % 0.063 W 0402
R515	1430778	Chip resistor		10 k	5 % 0.063 W 0402
R516	1430762	Chip resistor		2.2 k	5 % 0.063 W 0402
R518	1430804	Chip resistor		100 k	5 % 0.063 W 0402
R519	1430762	Chip resistor		2.2 k	5 % 0.063 W 0402
R520	1430804	Chip resistor		100 k	5 % 0.063 W 0402
R521	1430754	Chip resistor		1.0 k	5 % 0.063 W 0402
R523	1430762	Chip resistor		2.2 k	5 % 0.063 W 0402
R524	1430762	Chip resistor		2.2 k	5 % 0.063 W 0402
R525	1430726	Chip resistor		100	5 % 0.063 W 0402
R527	1430762	Chip resistor		2.2 k	5 % 0.063 W 0402
R528	1430762	Chip resistor		2.2 k	5 % 0.063 W 0402
R531	1430762	Chip resistor		2.2 k	5 % 0.063 W 0402
R532	1430754	Chip resistor		1.0 k	5 % 0.063 W 0402
R546	1430718	Chip resistor		47	5 % 0.063 W 0402
R570	1430770	Chip resistor		4.7 k	5 % 0.063 W 0402
R571	1430700	Chip resistor		10	5 % 0.063 W 0402
R572	1430732	Chip resistor		180	5 % 0.063 W 0402
R579	1430700	Chip resistor		10	5 % 0.063 W 0402
R581	1430740	Chip resistor		330	5 % 0.063 W 0402
R600	1430726	Chip resistor		100	5 % 0.063 W 0402
R603	1430770	Chip resistor		4.7 k	5 % 0.063 W 0402
R604	1430740	Chip resistor		330	5 % 0.063 W 0402
R605	1430730	Chip resistor		150	5 % 0.063 W 0402
R606	1430730	Chip resistor		150	5 % 0.063 W 0402
R610	1430778	Chip resistor		10 k	5 % 0.063 W 0402
R611	1430740	Chip resistor		330	5 % 0.063 W 0402
R612	1430778	Chip resistor		10 k	5 % 0.063 W 0402
R701	1430700	Chip resistor		10	5 % 0.063 W 0402
R703	1430770	Chip resistor		4.7 k	5 % 0.063 W 0402
R704	1430784	Chip resistor		15 k	5 % 0.063 W 0402
R706	1430762	Chip resistor		2.2 k	5 % 0.063 W 0402
R707	1430812	Chip resistor		220 k	5 % 0.063 W 0402
R708	1430700	Chip resistor		10	5 % 0.063 W 0402
R711	1430732	Chip resistor		180	5 % 0.063 W 0402
R712	1430778	Chip resistor		10 k	5 % 0.063 W 0402
R714	1430754	Chip resistor		1.0 k	5 % 0.063 W 0402
R715	1430726	Chip resistor		100	5 % 0.063 W 0402
R716	1430700	Chip resistor		10	5 % 0.063 W 0402
R717	1430762	Chip resistor		2.2 k	5 % 0.063 W 0402
R729	1430770	Chip resistor		4.7 k	5 % 0.063 W 0402

R755	1430716	Chip resistor	39	5 % 0.063 W 0402
R756	1430706	Chip resistor	15	5 % 0.063 W 0402
R757	1430716	Chip resistor	39	5 % 0.063 W 0402
R758	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R759	1430700	Chip resistor	10	5 % 0.063 W 0402
R760	1430740	Chip resistor	330	5 % 0.063 W 0402
C080	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C081	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C082	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C083	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C084	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C085	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C086	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C087	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C088	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C089	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C100	2610005	Tantalum cap.	10 u	20 % 16 V 3.5x2.8x1.9
C106	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C107	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C108	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C109	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C112	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C117	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C119	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C120	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C121	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C124	2610005	Tantalum cap.	10 u	20 % 16 V 3.5x2.8x1.9
C125	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C128	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C130	2320728	Ceramic cap.	220 p	10 % 50 V 0402
C136	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C138	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C139	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C140	2604127	Tantalum cap.	1.0 u	20 % 35 V 3.5x2.8x1.9
C145	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C147	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C148	2312403	Ceramic cap.	2.2 u	10 % 10 V 1206
C153	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C154	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C155	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C156	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C157	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C158	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C159	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C160	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C167	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C168	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C169	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C170	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C172	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C173	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C174	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805

C175	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C176	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C177	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C181	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C197	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402
C198	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C199	2320548	Ceramic cap.	33 p	5 % 50 V 0402
C200	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C201	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C203	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C204	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C205	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C206	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C207	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C209	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C211	2320469	Ceramic cap.		Y5 V 0603
C212	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C213	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C214	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C300	2312296	Ceramic cap.		Y5 V 1210
C301	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C302	2312296	Ceramic cap.		Y5 V 1210
C304	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C305	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C306	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C307	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C308	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C315	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C316	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C317	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C318	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C319	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C322	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C323	2610003	Tantalum cap.	10 u	20 % 10 V 3.2x1.6x1.6
C325	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C326	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C327	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C335	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C336	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C337	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C338	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C500	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C501	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C502	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C503	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C505	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C506	2610013	Tantalum cap.	220 u	10 % 10 V 7.3x4.3x4.1
C507	2610013	Tantalum cap.	220 u	10 % 10 V 7.3x4.3x4.1
C508	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C509	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C511	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C512	2320536	Ceramic cap.	10 p	5 % 50 V 0402

C513	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C514	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C515	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C516	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C517	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C518	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C519	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C520	2611668	Tantalum cap.	4.7 u	20 % 10 V 3.2x1.6x1.6
C521	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C522	2320564	Ceramic cap.	150 p	5 % 50 V 0402
C523	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C524	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C525	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C526	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C527	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C528	2320921	Ceramic cap.		25 V 0402
C530	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C531	2320576	Ceramic cap.	470 p	5 % 50 V 0402
C533	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C535	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C536	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C537	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402
C538	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C539	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C540	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C541	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C542	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C544	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402
C545	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C546	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C547	2320907	Ceramic cap.		25 V 0402
C549	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C561	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C562	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C563	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C564	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C600	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C601	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C602	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C603	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402
C604	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C605	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402
C606	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402
C609	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C611	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C612	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C613	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C614	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C616	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C617	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C618	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C619	2320592	Ceramic cap.	2.2 n	5 % 50 V 0402

C620	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C621	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C622	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C623	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C624	2320564	Ceramic cap.	150 p	5 % 50 V 0402
C640	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C641	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C666	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C671	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C700	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C703	2310248	Ceramic cap.	4.7 n	5 % 50 V 1206
C704	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C705	2320568	Ceramic cap.	220 p	5 % 50 V 0402
C706	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C707	2320576	Ceramic cap.	470 p	5 % 50 V 0402
C708	2310248	Ceramic cap.	4.7 n	5 % 50 V 1206
C709	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C710	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C711	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C714	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C716	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C718	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C719	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C720	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C721	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C722	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C728	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C730	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C734	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C735	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C760	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C761	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C762	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402
C771	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C772	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C773	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C774	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C775	2320546	Ceramic cap.	27 p	5 % 50 V 0402
L105	3203701	Ferrite bead 33r/100mhz	0805	0805
L109	3203701	Ferrite bead 33r/100mhz	0805	0805
L500	3645105	Chip coil 27 n	5 % Q=12/100 MHz	0603
L501	3645105	Chip coil 27 n	5 % Q=12/100 MHz 0603	
L502	3645105	Chip coil 27 n	5 % Q=12/100 MHz 0603	
L503	3645105	Chip coil 27 n	5 % Q=12/100 MHz 0603	
L601	3645105	Chip coil 27 n	5 % Q=12/100 MHz 0603	
L602	3645105	Chip coil 27 n	5 % Q=12/100 MHz 0603	
L603	3645183	Chip coil 56 n	5 % Q=12/100 MHz 0603	
L607	3645037	Chip coil 150 n	10 % Q=15/25 MHz 0603	
L608	3645037	Chip coil 150 n	10 % Q=15/25 MHz 0603	
L609	3645037	Chip coil 150 n	10 % Q=15/25 MHz 0603	
L610	3645179	Chip coil 2 n	Q=8/100M 0603	
L611	3645181	Chip coil 3 n	10 % Q=10/100 MHz 0603	

L701	3641206	Chip coil	10 % Q=25/7.96 MHz	1008
L703	3645129	Chip coil	18 n	5 % Q=8/100M 0603
B150	4510003	Crystal	32.768 k	+–20PPM 8x3.8
G701	4350095	Vco 1443–1510mhz 2.8v 12ma	pcs	PCS
G702	4350103	Vco 800mhz 2.8v 7ma		
G703	4510167	VCTCXO	13.0 M	+–5PPM 2.8V DCS
F100	5119019	SM, fuse f 1.5a 32v	0603	
Z100	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
Z101	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
Z102	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
Z103	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
Z104	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
Z401	4512011	Dupl 1850–1910/1930–1990Mhz 20x14		20x14
Z503	4511023	Saw filter	1880+–30 M	/4.2DB 3X3
Z505	4550031	Cer.filt 1880+–30Mhz	6.4x5.5	6.4x5.5
Z511	3640069	Filt 47pf 25v 0r01 6a	1206	
Z604	4550035	Cer.filt 1960+–30Mhz/2.		4DB7.7X4.
Z605	4511001	Saw filter	87+–0.12 M	
Z606	4510009	Cer.filt 13+–0.09Mhz	7.2x3.2	7.2x3.2
Z621	4511033	Saw filter	487+–0.2 M	/4.5DB 4X4
V104	4200877	Transistor	BCX51–16	pnp 45 V 1.5 A SOT89
V109	4110067	Schottky diode	MBR0520L	20 V 0.5 A SOD123
V111	4110072	Diode x 2	BAV99W	70 V 0.2 A SOT323
V112	4110072	Diode x 2	BAV99W	70 V 0.2 A SOT323
V113	4110072	Diode x 2	BAV99W	70 V 0.2 A SOT323
V115	4110079	Schottky diode x 2	HSMS282C	15 V SOT323
V300	4210100	Transistor	BC848W	npn 30 V SOT323
V501	4110079	Sch. diode x 2	HSMS282C	15 V SOT323
V502	4110072	Diode x 2	BAV99W	70 V 0.2 A SOT323
V504	4210119	Transistor BC849CW	npn 30 V 0.1 A	SOT323
V505	4210052	Transistor	DTC114EE	npn RB V EM3
V506	4202671	MosFet BST82	n–ch 80 V 175 mA	SOT23
V507	4210052	Transistor	DTC114EE	npn RB V EM3
V508	4112451	Pindiode bar63–03w 50v 0.1a sod323		SOD323
V509	4210052	Transistor	DTC114EE	npn RB V EM3
V510	4210074	Transistor	BFP420	npn 4. V SOT343
V511	4210052	Transistor	DTC114EE	npn RB V EM3
V600	4210015	Transistor	BFP405	npn 4. V SOT343
V710	4210100	Transistor	BC848W	npn 30 V SOT323
V720	4210074	Transistor	BFP420	npn 4. V SOT343
D100	4340387	IC, 2xbilateral switch sso	TC7W66FU	SSOP8
D200	4370279	Mad2 rom3 f711604 c12		TQFP176
D210	4340261	IC, flash mem.		TSO48
D221	4340273	IC, SRAM		STSOP32
D230	4342264	IC, EEPROM		SO8S
N100	4370047	Ccont 2f dct3 bb asic		TQFP64
N110	4370165	Chaps charger control	so16	SO16
N200	4340413	IC, regulator	TK11230BMC	3.0 V SOT23L
N300	4370317	Cobba_gj b07 bb asic dct3		TQFP64
N401	4370273	Plussa txmod+rxif+2pll		TQFP64
N402	4370245	Crfu2a_v3 comrfunit >2.7v		TSSOP28
N500	4370277	Rf9113 pw amp 1900mhz		PSOP2–16

N501	4340389	Bcr400w bias controller sot343	SOT343
S080	5219005	IC, SWsp–no 30vdc 50ma smSW TACT	SMD
S081	5219005	IC, SWsp–no 30vdc 50ma smSW TACT	SMD
X099	5460021	SM, conn 2x14m spring p1.0 pcb/p	PCB/PCB
X101	5469069	SM, batt conn 2pol spr p3.5 100v	100V2A
X102	5469069	SM, batt conn 2pol spr p3.5 100v	100V2A
X131	5469061	SM, system conn 6af+3dc+mic+jack	
X150	5400085	Sim card reader 2x3pol p2.54 sm	SM
X451	5429007	SM, coax conn m sw 50r 0.4–2ghz	
A500	9517013	SM, d rf shield pa–can dmc00455	
I001	9380753	Bar code label dmd03311 27x6.5	27x6.5
	9854170	PCB UR4_24 41.0X123.25X1.0 M6	4/P

This page intentionally left blank.